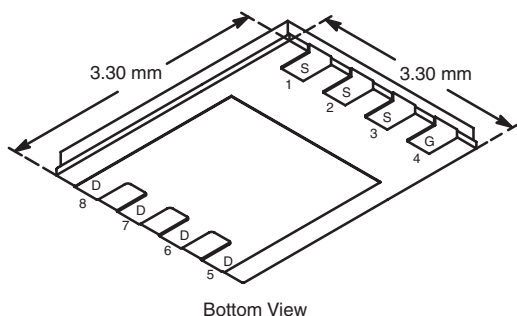


N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^f	Q_g (Typ.)
30	0.006 at $V_{GS} = 10$ V	35 ^g	13.7 nC
	0.0082 at $V_{GS} = 4.5$ V	35 ^g	

PowerPAK 1212-8



Bottom View

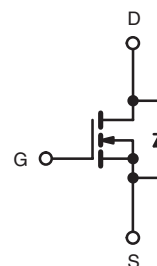
Ordering Information: Si7718DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- PWM Optimized
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- High Side Switch
- VRM
- POL



N-Channel MOSFET


RoHS
COMPLIANT

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	70	A
Continuous Source-Drain Diode Current	I_S	35 ^g	
		3.3 ^{a, b}	
Single Pulse Avalanche Current	I_{AS}	20	mJ
Single Pulse Avalanche Energy	E_{AS}	20	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, e}	R_{thJA}	24	33	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.4	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t = 10$ s.

c. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Maximum under steady state conditions is 81 °C/W.

f. Based on $T_C = 25$ °C.

g. Package limited.

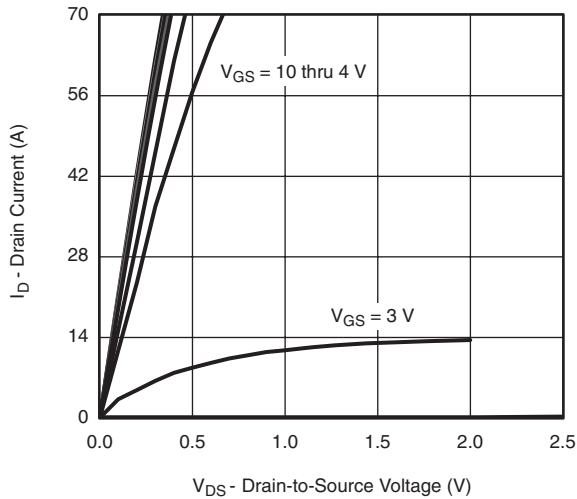
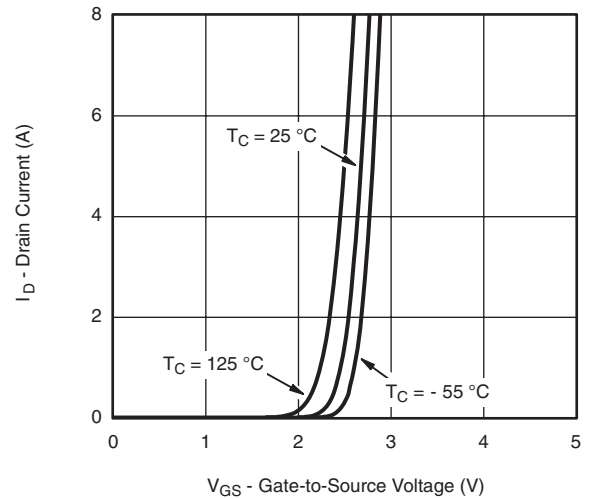
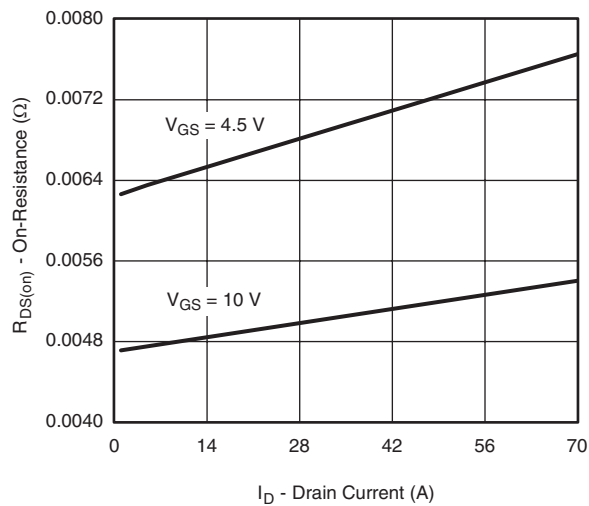
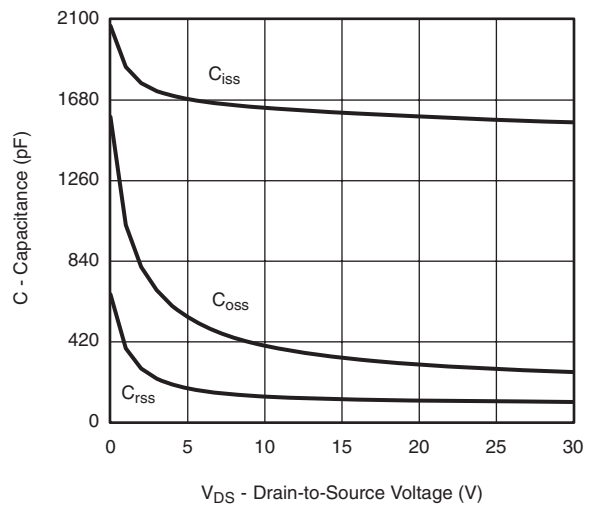
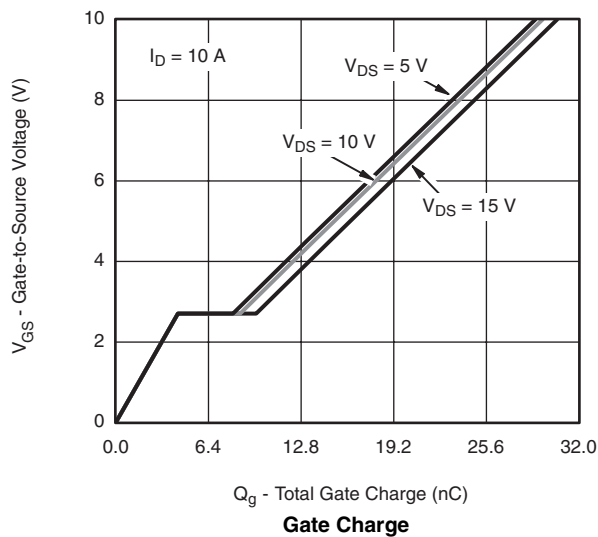
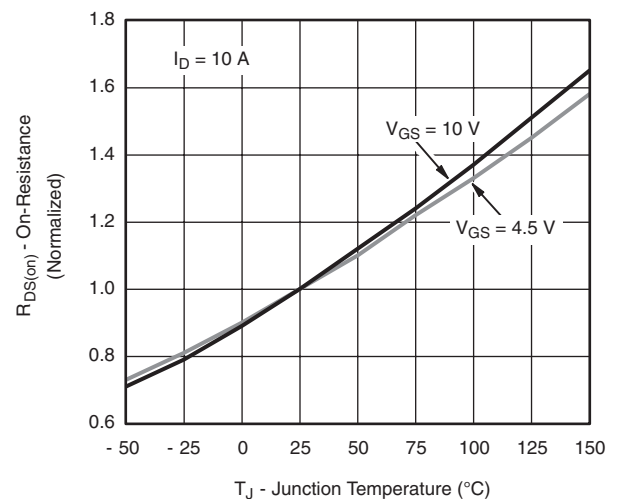
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		30		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		0.0048	0.006	Ω	
		V _{GS} = 4.5 V, I _D = 7 A		0.0065	0.0082		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		50		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1600		pF	
Output Capacitance	C _{oss}			335			
Reverse Transfer Capacitance	C _{rss}			115			
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		30	45	nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A		13.7	21		
Gate-Drain Charge	Q _{gd}			4.3			
Gate Resistance	R _g			4.3			
Turn-On Delay Time	t _{d(on)}	f = 1 MHz	0.3	0.75	1.5	Ω	
Rise Time	t _r		V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		22	35	ns
Turn-Off Delay Time	t _{d(off)}				13	26	
Fall Time	t _f				26	45	
Turn-On Delay Time	t _{d(on)}			12	24		
Rise Time	t _r	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		13	26		
Turn-Off Delay Time	t _{d(off)}			9	18		
Fall Time	t _f			22	35		
				8	16		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			35	A	
Pulse Diode Forward Current	I _{SM}				70		
Body Diode Voltage	V _{SD}	I _S = 3 A, V _{GS} = 0 V		0.75	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		19	35	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			9.5	18	nC	
Reverse Recovery Fall Time	t _a			11		ns	
Reverse Recovery Rise Time	t _b			8			

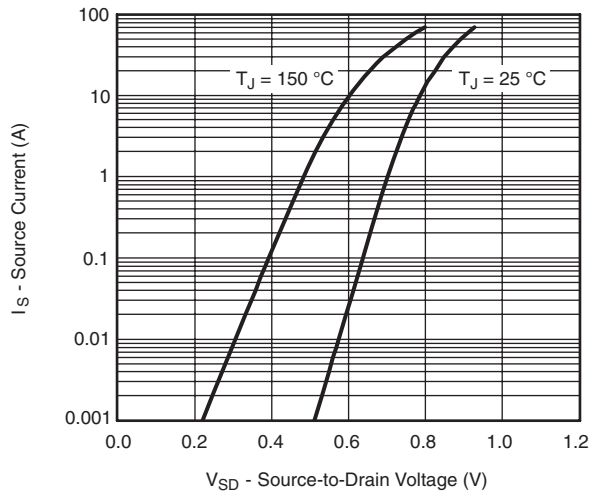
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

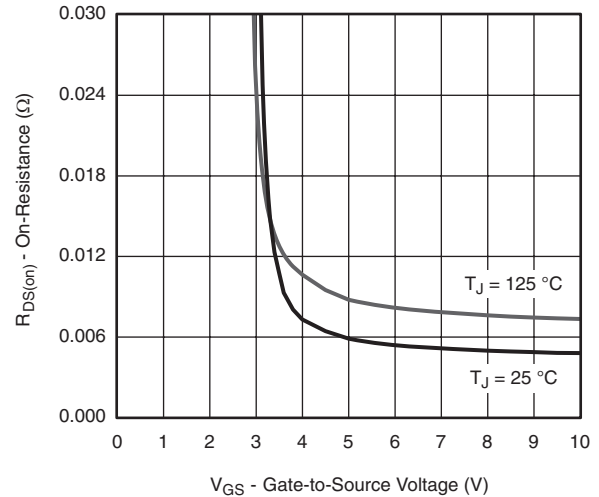
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

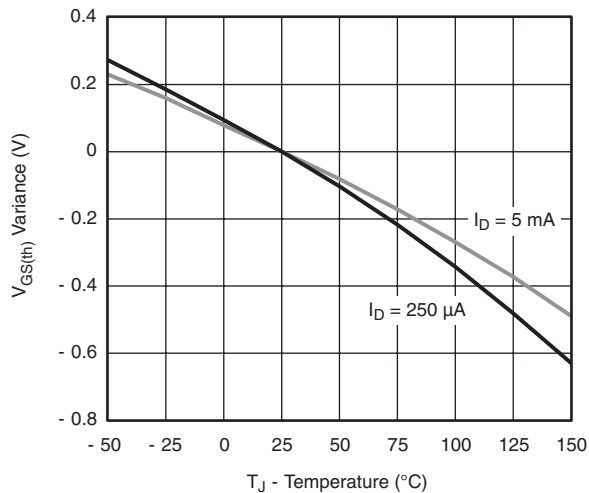
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

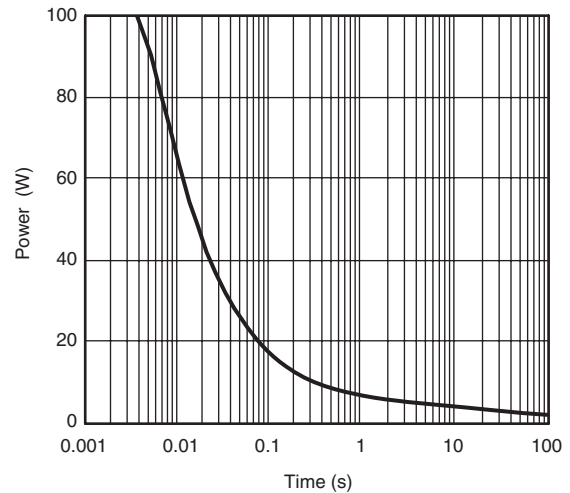
Source-Drain Diode Forward Voltage



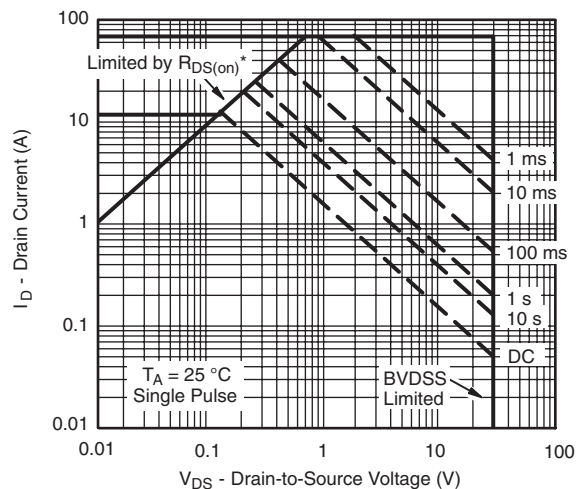
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



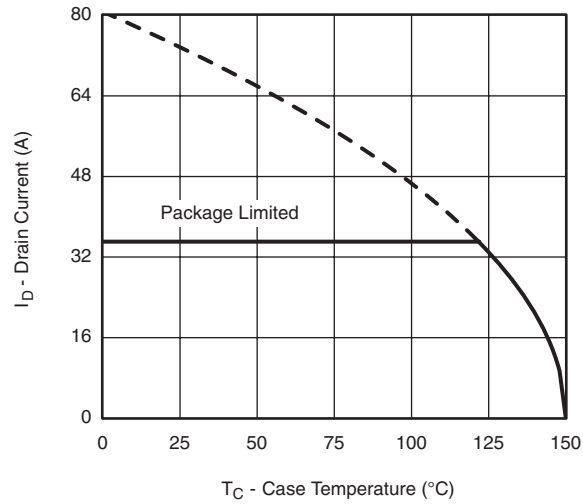
Single Pulse Power, Junction-to-Ambient

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

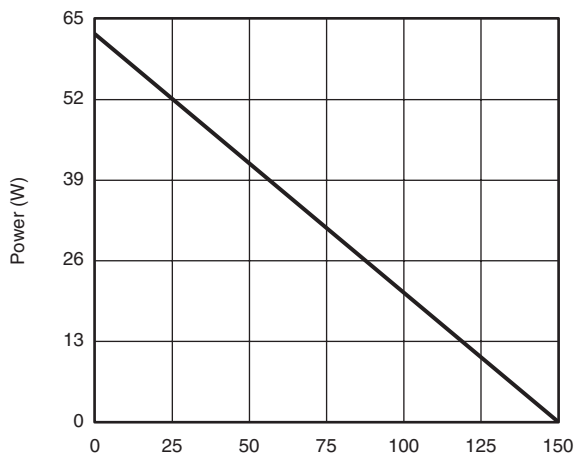
Safe Operating Area, Junction-to-Ambient



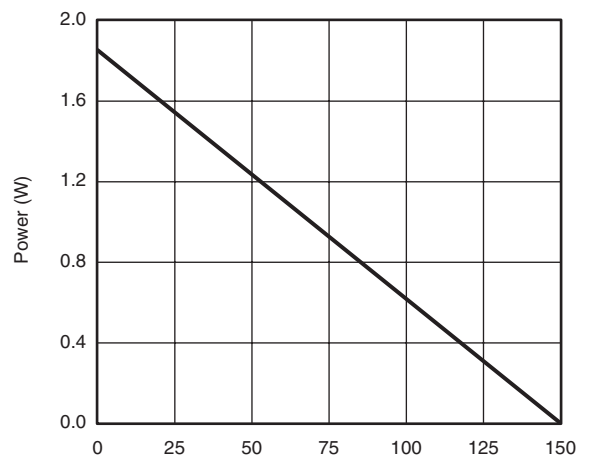
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*

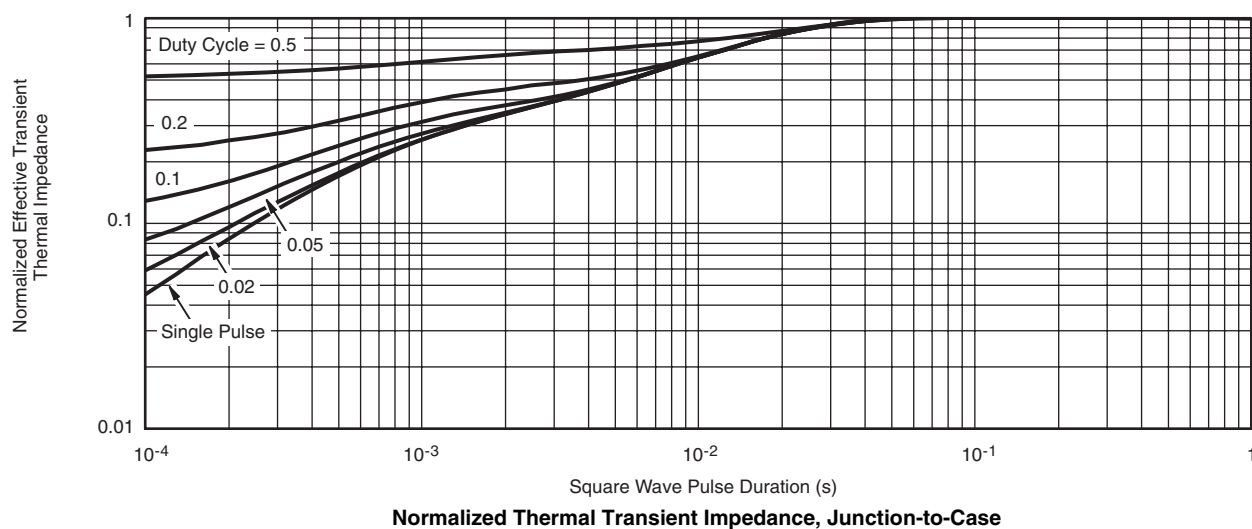
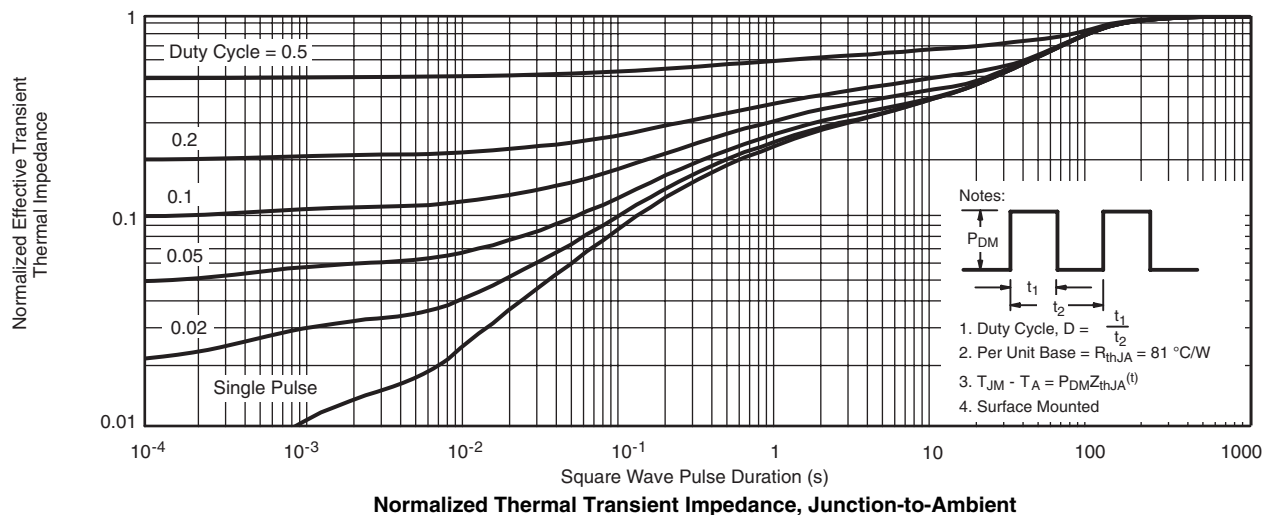


Power, Junction-to-Case



Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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