LM2902

Low power quad operational amplifier

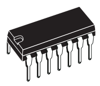
Features

- Wide gain bandwidth: 1.3MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100dB
- Very low supply current per amp: 375µA
- Low input bias current: 20nA
- Low input offset current: 2nA
- Wide power supply range:
  - Single supply: +3V to +30V
  - Dual supplies: ±1.5V to ±15V

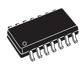
Description

This circuit consists of four independent, high gain, internally frequency compensated operational amplifiers designed especially for automotive and industrial control systems.

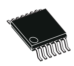
It operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.



N
DIP14
(Plastic package)



D
SO-14
(Plastic micropackage)



P
TSSOP14
(Thin shrink small outline package)

1 Schematic diagram

Figure 1. Schematic diagram (1/4 LM2902)

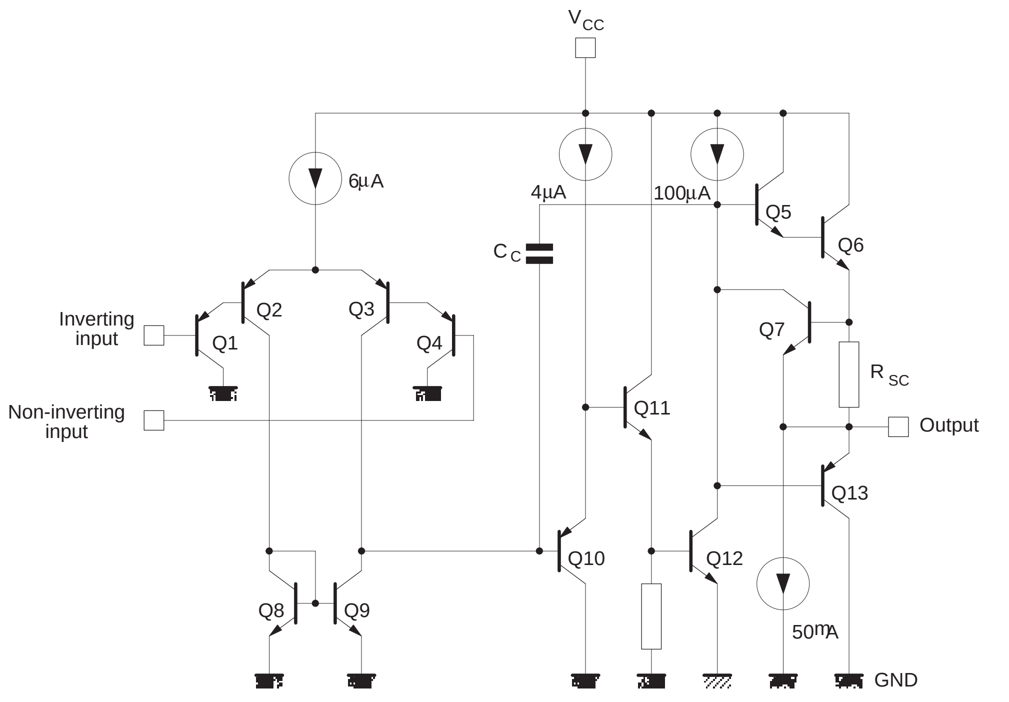
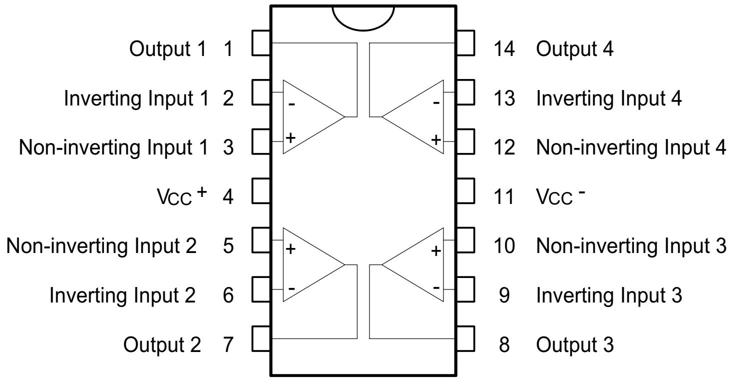


Figure 2. Pin connections (top view)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	±16 to 33	V
V_{ID}	Differential input voltage (2)	+32	V
V_{in}	Input voltage	-0.3 to +32	V
	Output short-circuit duration (3)	Infinite	s
P_d	Power dissipation (4) DIP14 SO-14	 500 400	mW
I_{in}	Input current (5)	50	mA
T_{stg}	Storage temperature range	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient SO-14 TSSOP14 DIP14	 105 100 80	°C/W
R_{thjc}	Thermal resistance junction to case SO-14 TSSOP14 DIP14	 31 32 33	°C/W
ESD	HBM: human body model(6)	370	V
	MM: machine model(7)	150	V
	CDM: charged device model(8)	1500	V

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA, independent of the magnitude of V_{CC}^+.
4. Pd is calculated with T_{amb} = +25°C, T_j = +150°C.
5. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
6. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range	V_{CC}^{+} - 1.5	V
T_{oper}	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. V_{CC}^+ = 5V, V_{CC}^- = Ground, V_o = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		2	7 9	mV
I_{io}	Input offset current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		2	30 40	nA
I_{ib}	Input bias current (2) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		20	150 300	nA
A_{vd}	Large signal voltage gain V_{CC}^+ = +15V, R_L=2kΩ, V_o = 1.4V to 11.4V T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_S \leq$10kΩ) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	65 65	110		dB
I_{cc}	Supply current, all amps, no load T_{amb} = +25°C, V_{CC} = +5V V_{CC} = +30V $T_{min} \leq T_{amb} \leq T_{max}$, V_{CC} = +5V V_{CC} = +30V		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input common mode voltage range (V_{CC}= +30V)(3) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common-mode rejection ratio ($R_S \leq$ 10kΩ) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	70 60	80		dB
I_O	Output short-circuit current (V_{id} = +1V) V_{CC} = +15V, V_o = +2V	20	40	70	mA
I_{sink}	Output sink current (V_{id} = -1V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		mA µA
V_{OH}	High level output voltage (V_{CC} = +30V) T_{amb} = +25°C, R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = +25°C, R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$ V_{CC} = +5V, R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = +25°C	26 26 27 27 3.5 3	27 28		V

Table 3. $V_{CC}^{+} = 5V$, V_{CC}^{-} = Ground, $V_o = 1.4V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage ($R_L = 10k\Omega$) $T_{amb} = +25°C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew rate $V_{CC} = 15V$, $V_{in} = 0.5$ to $3V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity gain		0.4		V/µs
GBP	Gain bandwidth product $V_{CC} = 30V$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$		1.3		MHz
THD	Total harmonic distortion $f = 1kHz$, $A_V = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{pp}$, $C_L = 100pF$, $V_{CC} = 30V$		0.015		%
e_n	Equivalent input noise voltage $f = 1kHz$, $R_S = 100\Omega$, $V_{CC} = 30V$		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	200	pA/°C
V_{O1}/V_{O2}	Channel separation (4) $1kHz \leq f \leq 20kHz$		120		dB

1. $V_O = 1.4V$, $R_S = 0\Omega$, $5V < V_{CC}^{+} < 30V$, $0V < V_{ic} < V_{CC}^{+} - 1.5V$.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^{+} –1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components ensure stray capacitance does not cause coupling between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Figure 3. Input bias current vs. T_{amb}

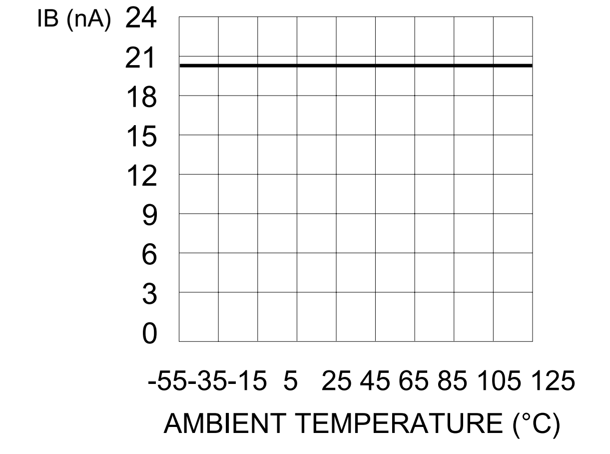


Figure 4. Input voltage range

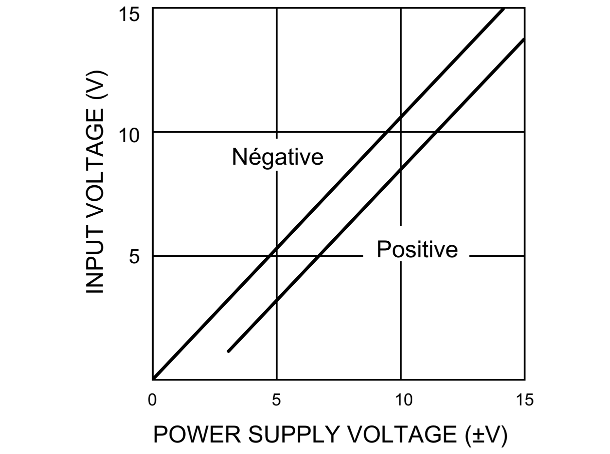


Figure 5. Current limiting

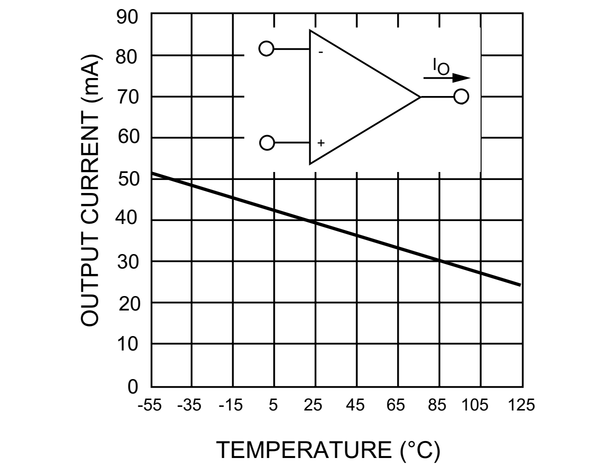


Figure 6. Supply current

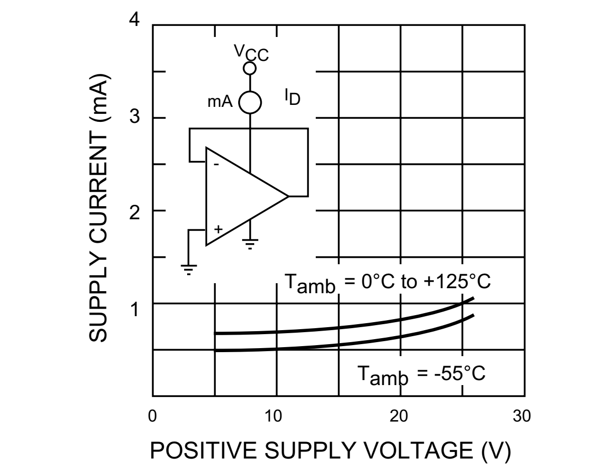


Figure 7. Gain bandwidth product

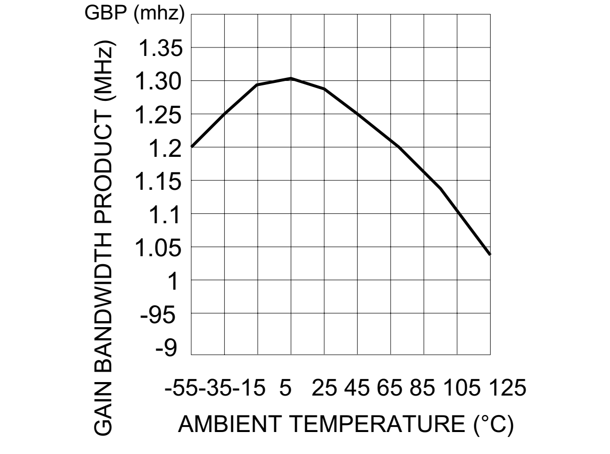


Figure 8. Voltage follower pulse response

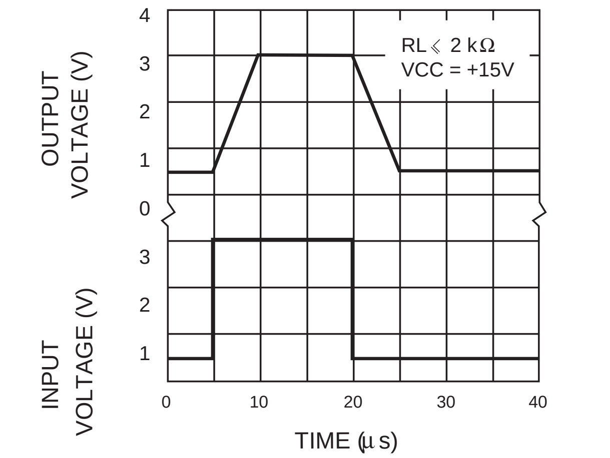


Figure 9. Common mode rejection ratio

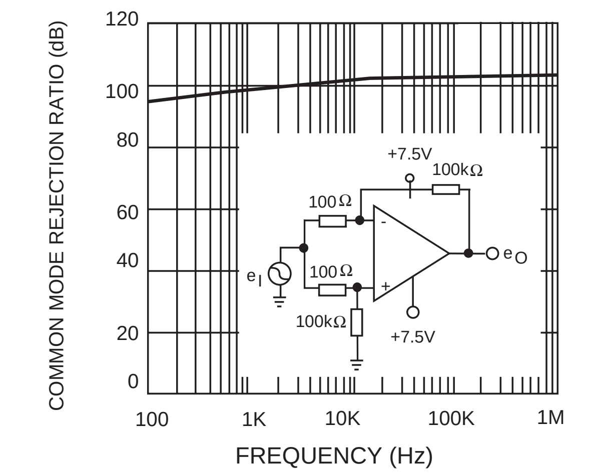


Figure 10. Output characteristics

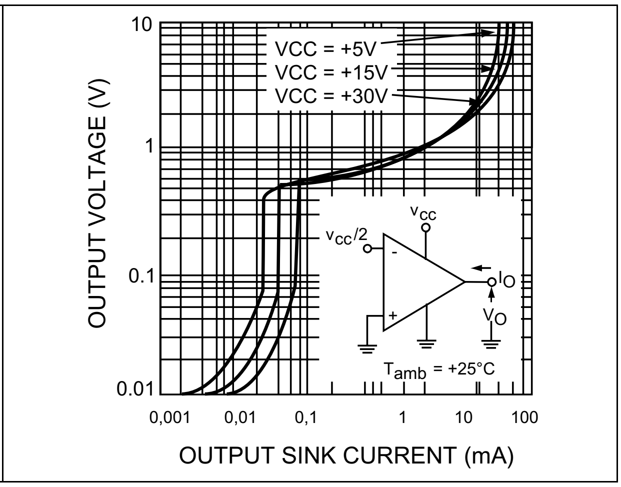


Figure 11. Open loop frequency response

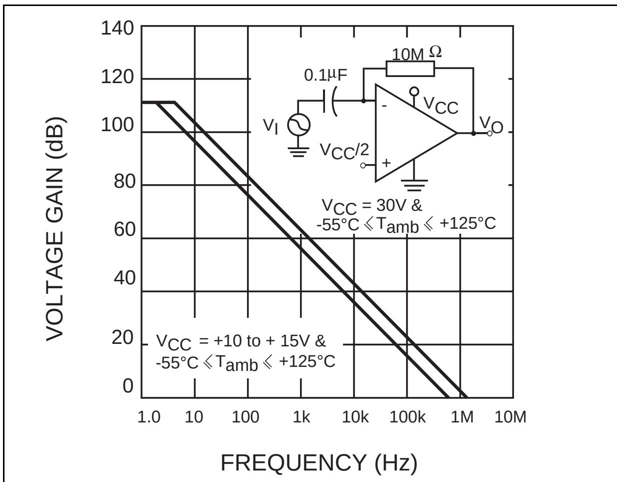


Figure 12. Voltage follower pulse response

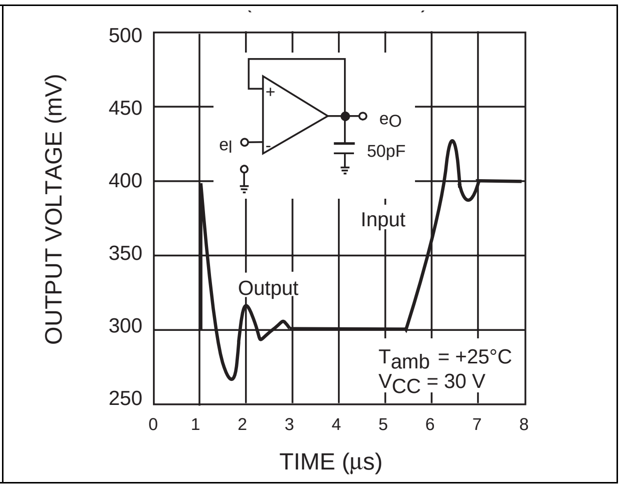


Figure 13. Large signal frequency response

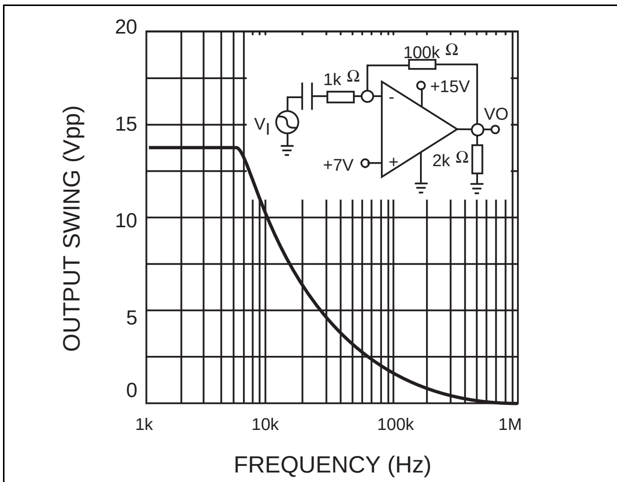


Figure 14. Output characteristics

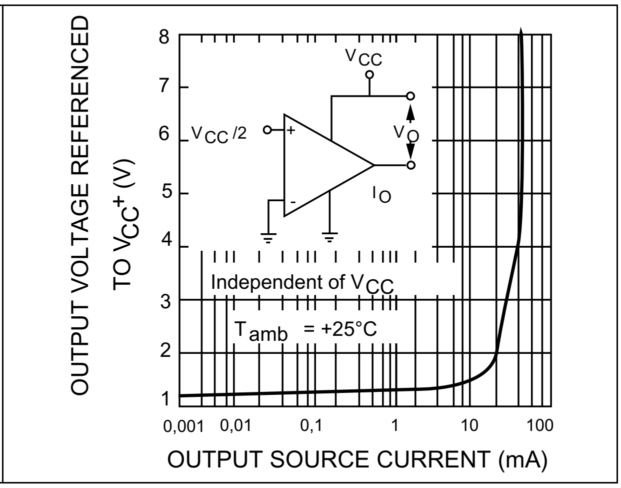


Figure 15. Input current

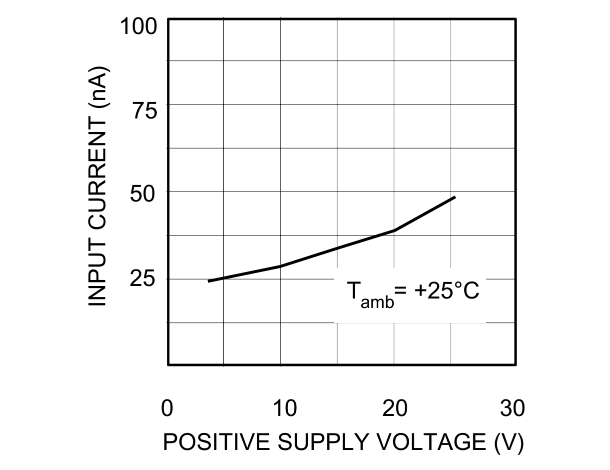


Figure 16. Voltage gain

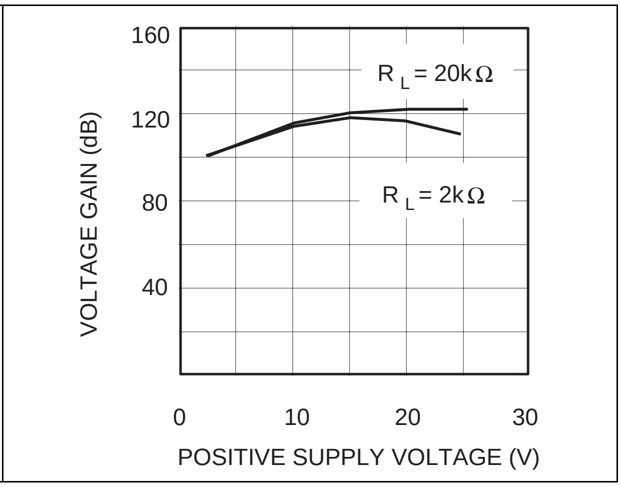


Figure 17. Power supply and common mode rejection ration

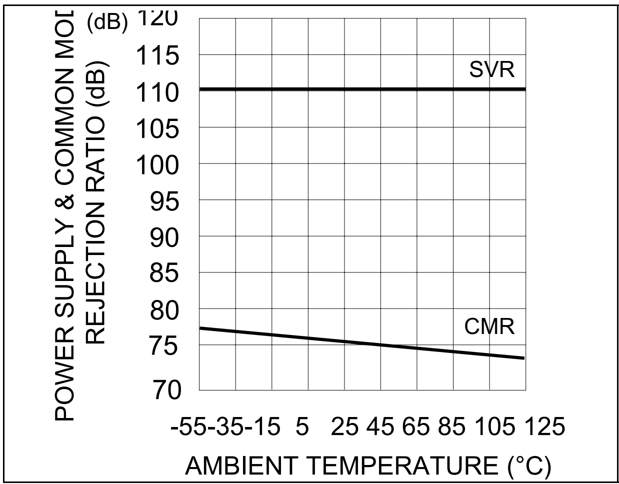
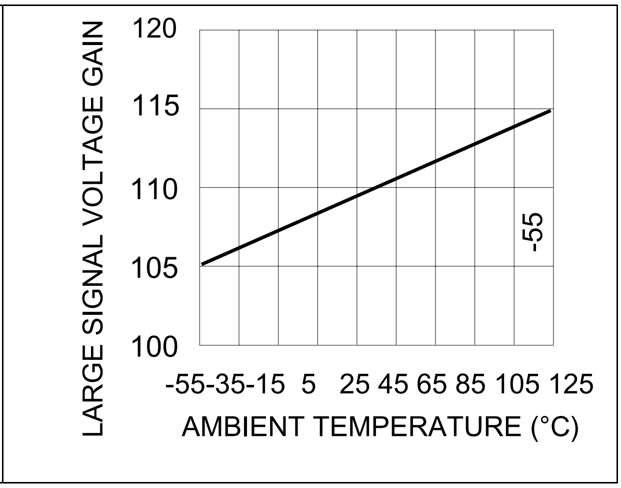


Figure 18. Large signal voltage gain



4 Typical single-supply applications

Figure 19. AC coupled inverting amplifier

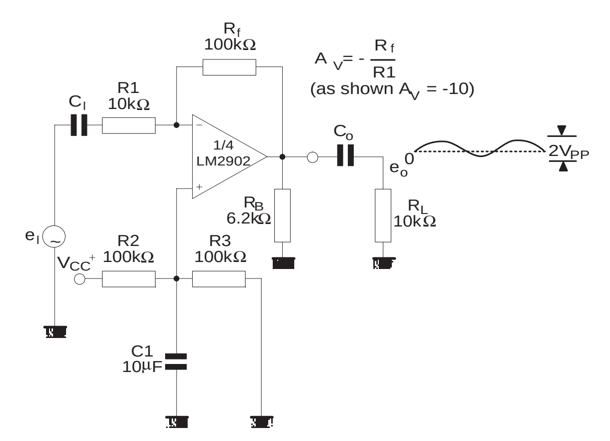


Figure 20. AC coupled non-inverting amplifier

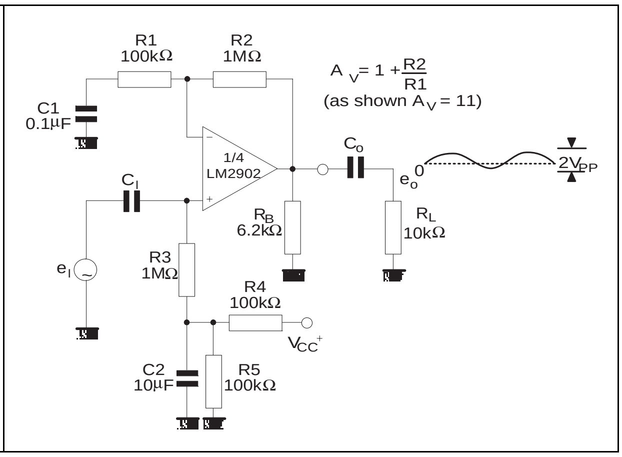


Figure 21. Non-inverting DC gain

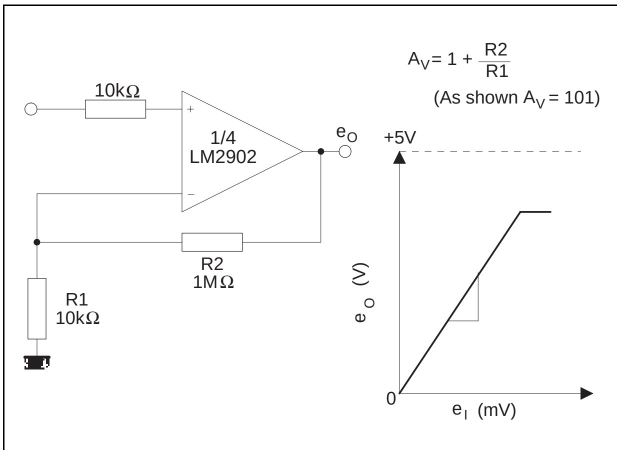


Figure 22. DC summing amplifier

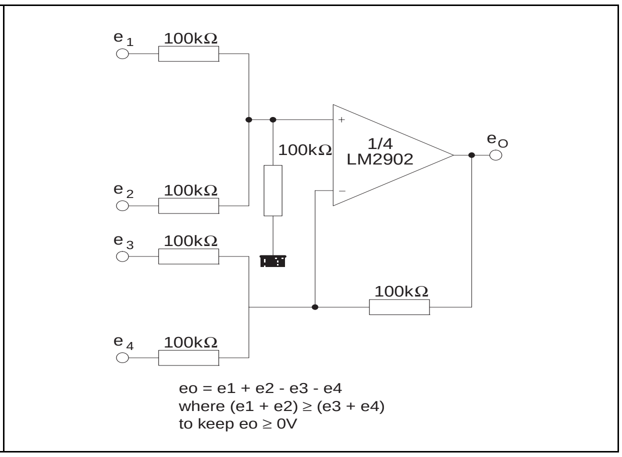


Figure 23. Active bandpass filter

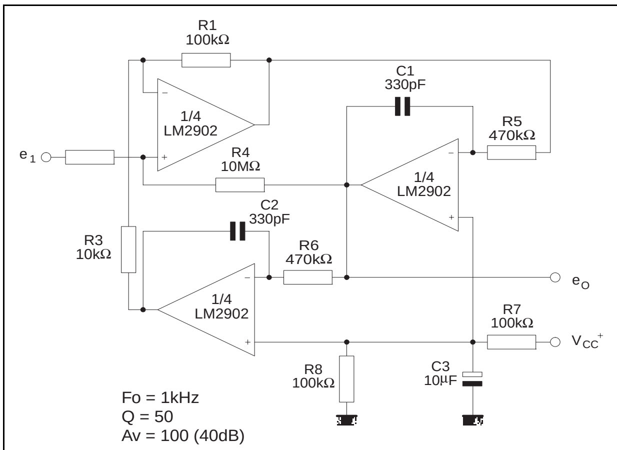


Figure 24. High input Z adjustable gain DC instrumentation amplifier

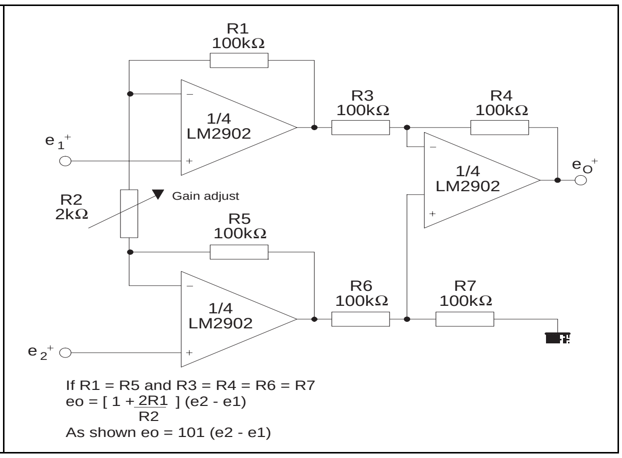


Figure 25. High input Z, DC differential amplifier

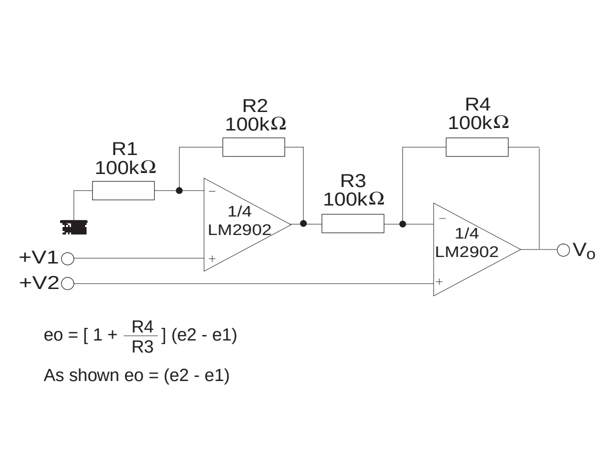


Figure 26. Low drift peak detector

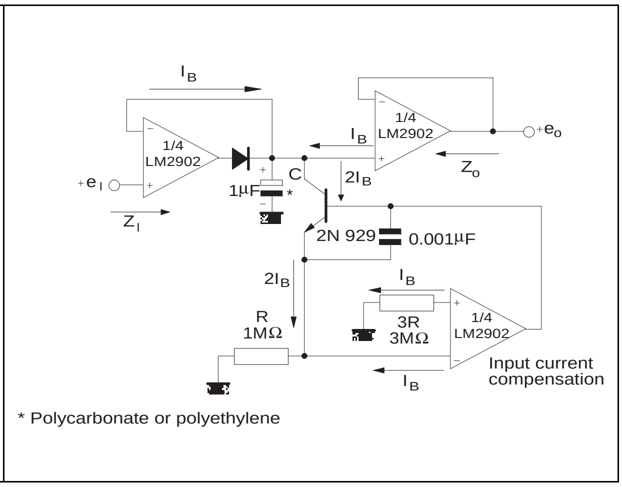
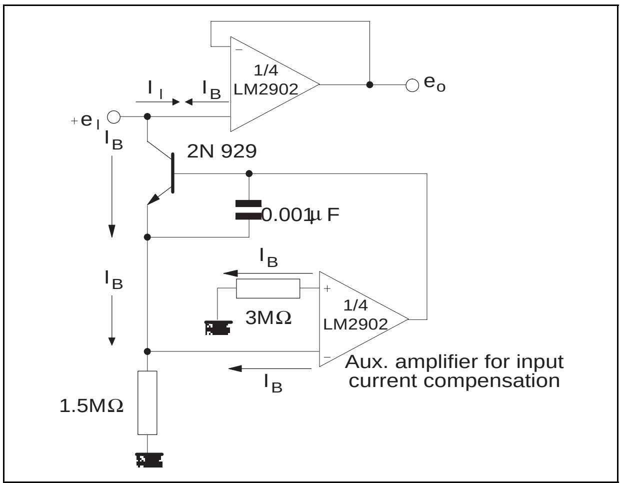


Figure 27. Using symmetrical amplifiers to reduce input current (general concept)



5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 28. DIP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

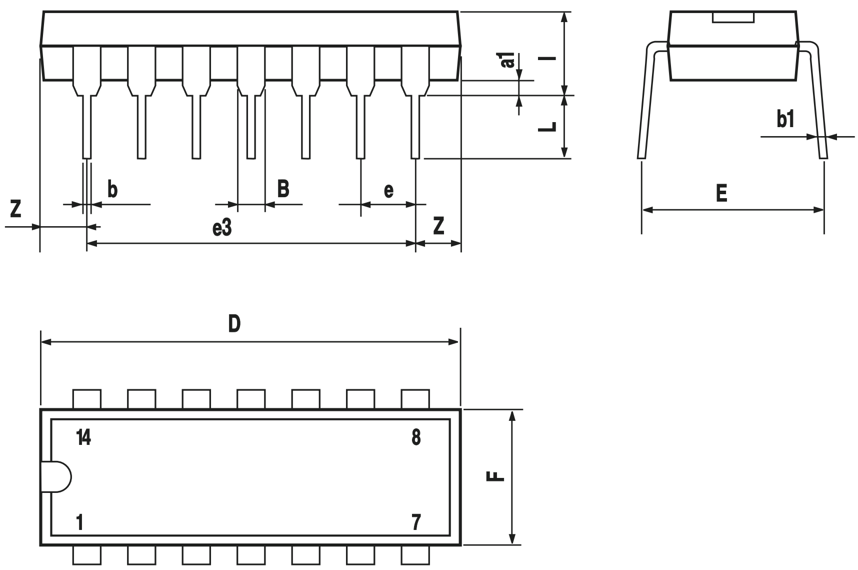


Figure 29. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

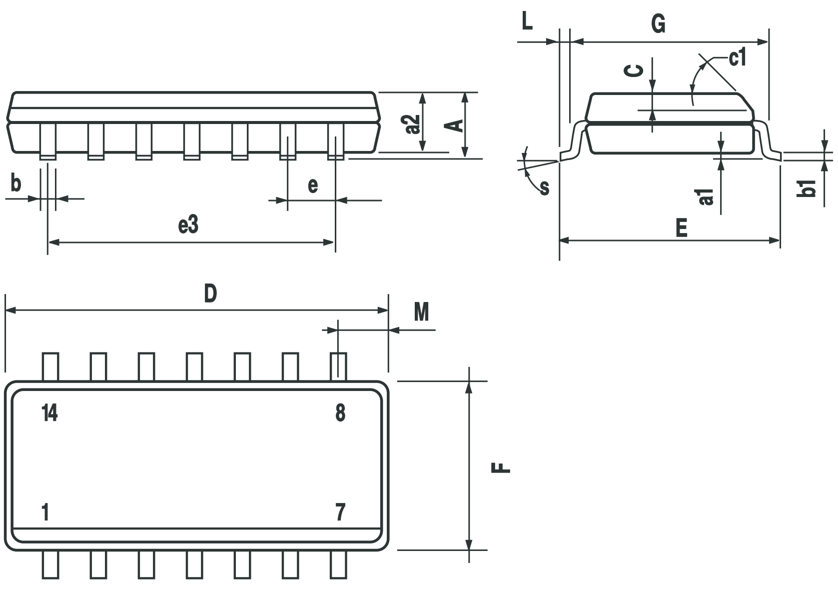
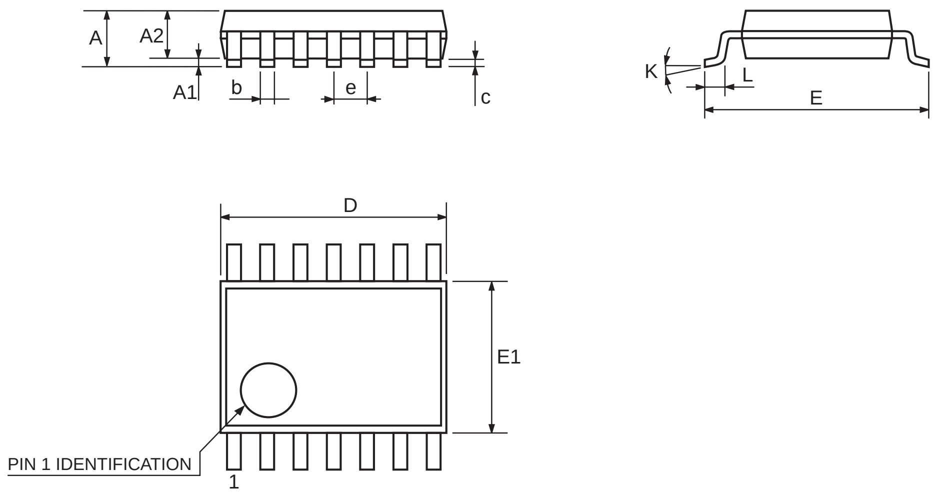


Figure 30. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



6 Ordering information

Table 4. Order codes

<table>
<tr><th>Part number</th><th>Temperature range</th><th>Package</th><th>Packing</th><th>Marking</th></tr>
<tr><td>LM2902N</td><td rowspan="5">-40°C, +125°C</td><td>DIP14</td><td>Tube</td><td>LM2902N</td></tr>
<tr><td>LM2902D
LM2902DT</td><td>SO-14</td><td>Tube or
tape & reel</td><td rowspan="2">2902</td></tr>
<tr><td>LM2902PT</td><td>TSSOP14
(Thin shrink outline package)</td><td>Tape & reel</td></tr>
<tr><td>LM2902YD
LM2902YDT(1)</td><td>SO-14
(Automotive grade level)</td><td>Tube or
tape & reel</td><td rowspan="2">2902Y</td></tr>
<tr><td>LM2902YPT(1)</td><td>TSSOP14
(Automotive grade level)</td><td>Tape & reel</td></tr>
</table>

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

7 Revision history

Date	Revision	Changes
30-Nov-2001	1	Initial release.
1-Jul-2005	2	PPAP references inserted in the datasheet, see *Table 4: Order codes*. ESD protection inserted in *Table 1 on page 3*.
31-Oct-2005	3	An error in the device description was corrected on page 1. PPAP reference inserted in the datasheet see *Table 4: Order codes*. Minor grammatical and formatting changes throughout.
18-Jun-2007	4	Values for themal resistance junction to ambient and ESD HBM corrected in *Table 1: Absolute maximum ratings (AMR)*. Values for themal resistance junction to case added in *Table 1: Absolute maximum ratings (AMR)*. *Table 2: Operating conditions* added. Electrical characteristics figure captions updated. *Section 5: Package information* updated. *Table 4: Order codes* moved to end of document.