



IRF730

N-channel 400V - 0.75 Ω - 5.5A TO-220
Powermesh™II Power MOSFET

General features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|--------|------------------|---------------------|----------------|
| IRF730 | 400V | <1 Ω | 5.5A |

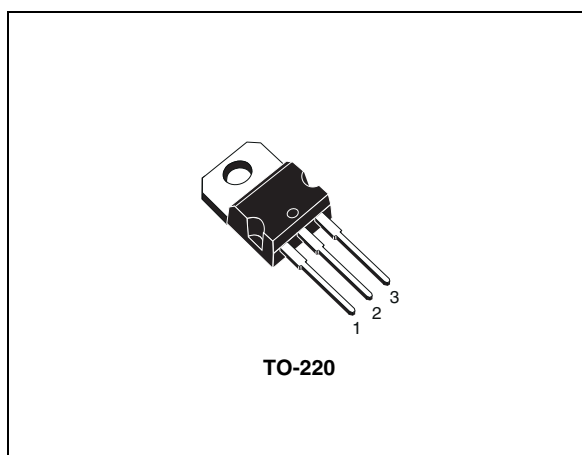
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Description

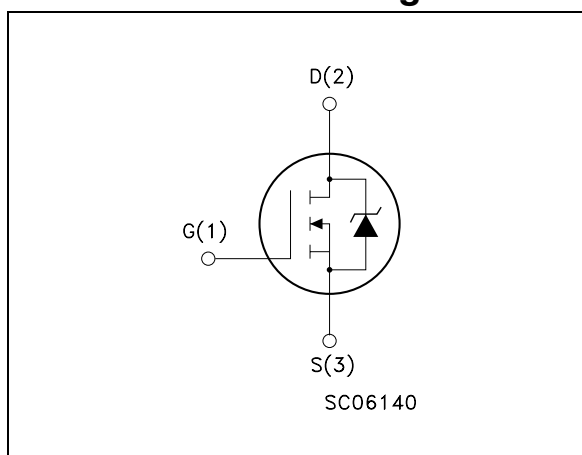
The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

Applications

- Switching application



Internal schematic diagram



Order codes

| Part number | Marking | Package | Packaging |
|-------------|---------|---------|-----------|
| IRF730 | IRF730 | TO-220 | Tube |

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1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|---------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 400 | V |
| V_{DGR} | Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$) | 400 | V |
| V_{GS} | Gate- source voltage | ± 20 | V |
| I_D | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 5.5 | A |
| I_D | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 3.5 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 22 | A |
| P_{TOT} | Total dissipation at $T_C = 25^\circ\text{C}$ | 100 | W |
| | Derating factor | 0.8 | W/ $^\circ\text{C}$ |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 3 | V/ns |
| T_{stg} | Storage temperature | -65 to 150 | $^\circ\text{C}$ |
| T_j | Max. operating junction temperature | 150 | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 5.5\text{A}$, $di/dt \leq 90\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{jmax}$.

Table 2. Thermal data

| | | | |
|-----------|--|------|---------------------------|
| Rthj-case | Thermal resistance junction-case max | 1.25 | $^\circ\text{C}/\text{W}$ |
| Rthj-amb | Thermal resistance junction-ambient max | 62.5 | $^\circ\text{C}/\text{W}$ |
| Rthc-sink | Thermal resistance case-sink typ | 0.5 | $^\circ\text{C}/\text{W}$ |
| T_l | Maximum lead temperature for soldering purpose | 300 | $^\circ\text{C}$ |

Table 3. Avalanche characteristics

| Symbol | Parameter | Max Value | Unit |
|----------|---|-----------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 5.5 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$) | 300 | mJ |

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 250 \mu\text{A}$, $V_{GS} = 0$ | 400 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125^{\circ}\text{C}$ | | | 1 50 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{V}$, $I_D = 3 \text{A}$ | | 0.75 | 1 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|------|-----------------|------|----------------------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 3 \text{A}$ | 2.9 | | | S |
| C_{iss} C_{oss} C_{rss} | Input capacitance Output capacitance Reverse transfer capacitance | $V_{DS} = 25\text{V}$, $f = 1 \text{MHz}$, $V_{GS} = 0$ | | 530 90 15 | | pF pF pF |
| $t_{d(on)}$ t_r $t_{d(off)}$ t_f | Turn-on delay time Rise time Off-voltage rise time Fall time | $V_{DD} = 200\text{V}$, $I_D = 3\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ | | 11 15 | | ns ns ns ns |
| Q_g Q_{gs} Q_{gd} | Total gate charge Gate-source charge Gate-drain charge | $V_{DD} = 320\text{V}$, $I_D = 5.5\text{A}$, $V_{GS} = 10\text{V}$ | | 18 4 8.5 | 24 | nC nC nC |

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 6. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|------------------|---------|--------------------|
| I_{SD} $I_{SDM}^{(1)}$ | Source-drain current Source-drain current (pulsed) | | | | 6 24 | A A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 5.5A, V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD} = 7A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_j = 150^\circ C$ | | 280 1.4 10 | | ns μC A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

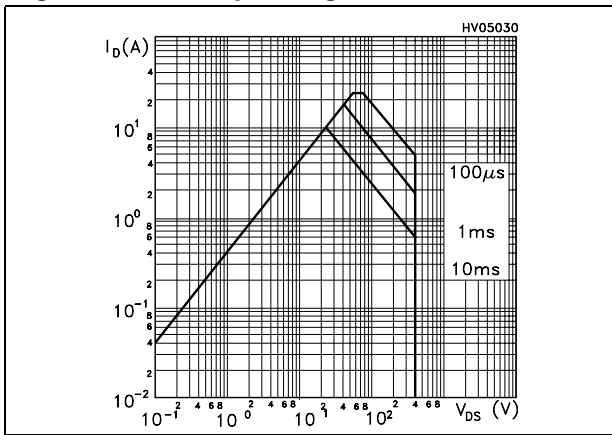


Figure 2. Thermal impedance

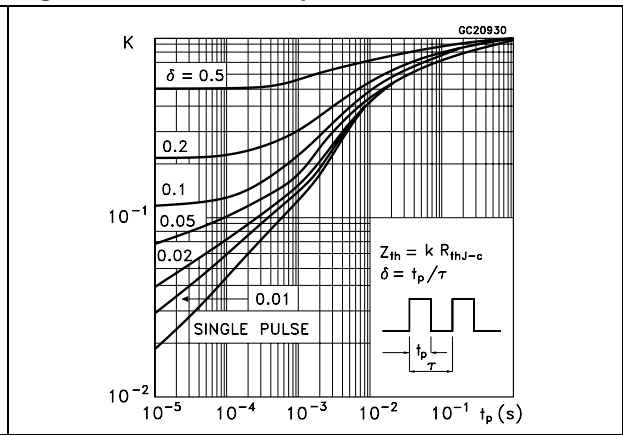


Figure 3. Output characteristics

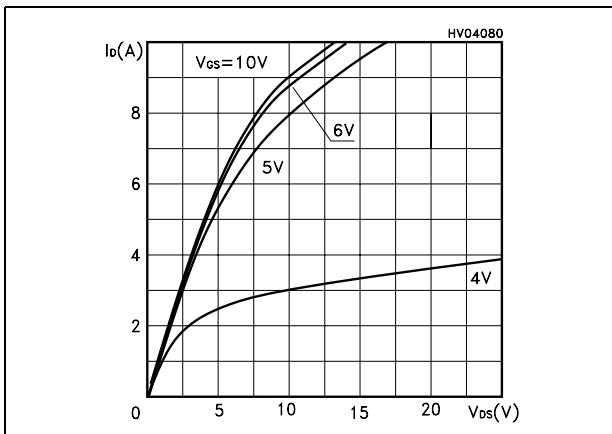


Figure 4. Transfer characteristics

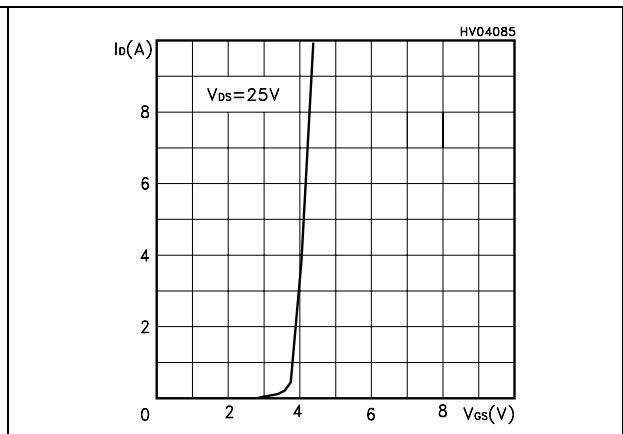


Figure 5. Transconductance

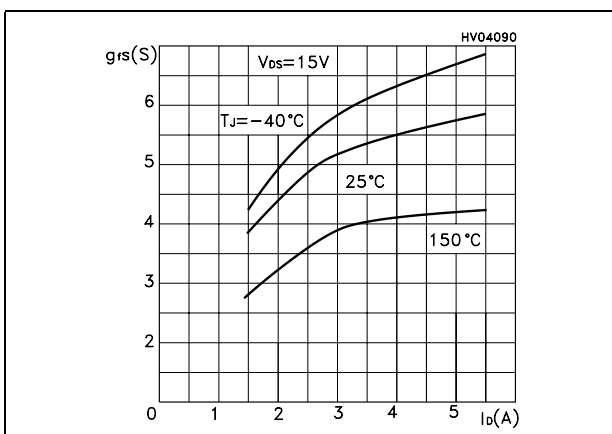


Figure 6. Static drain-source on resistance

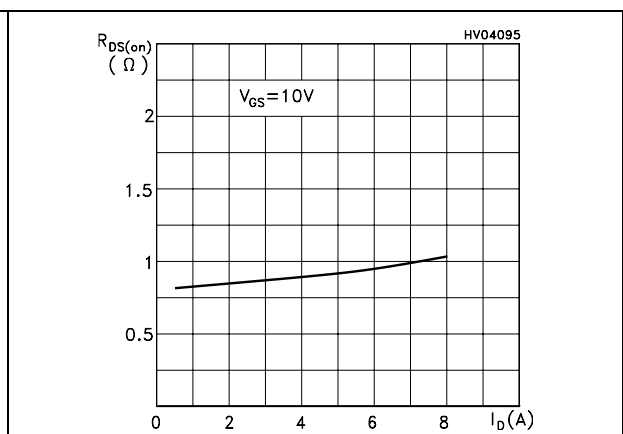


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

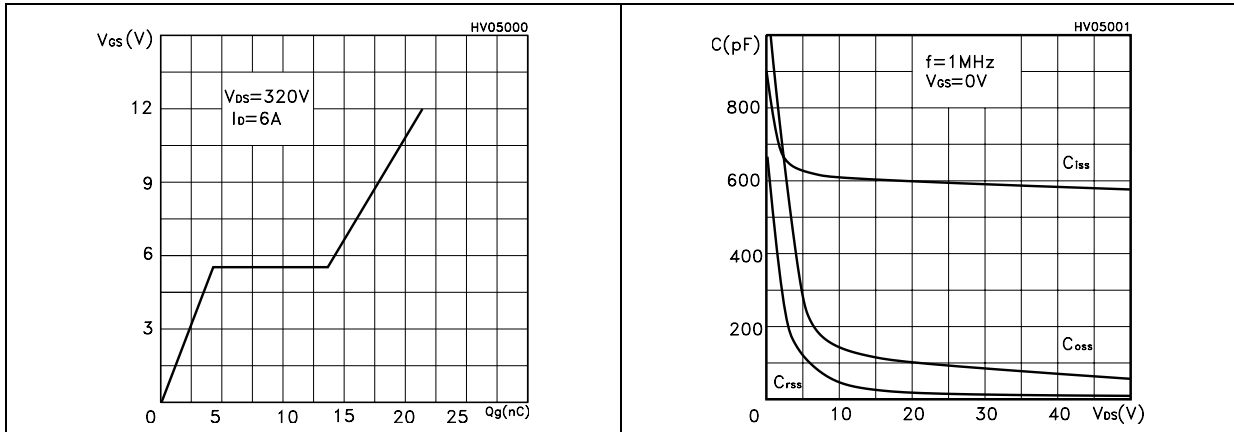


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

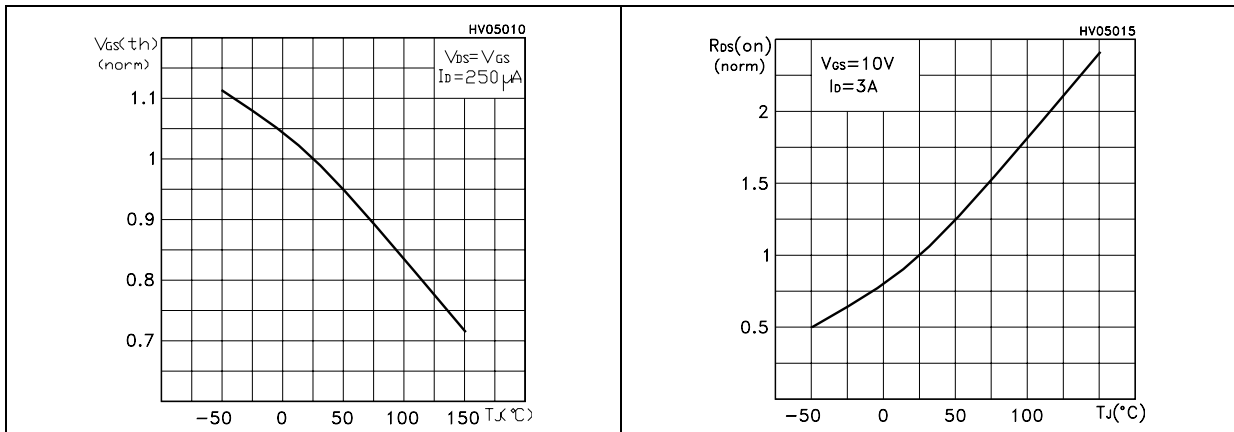
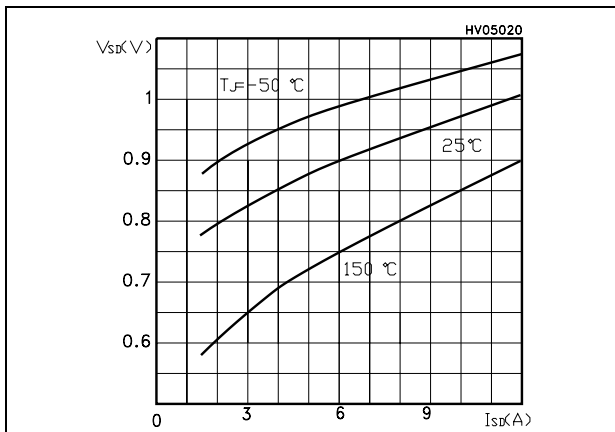


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Unclamped Inductive load test circuit

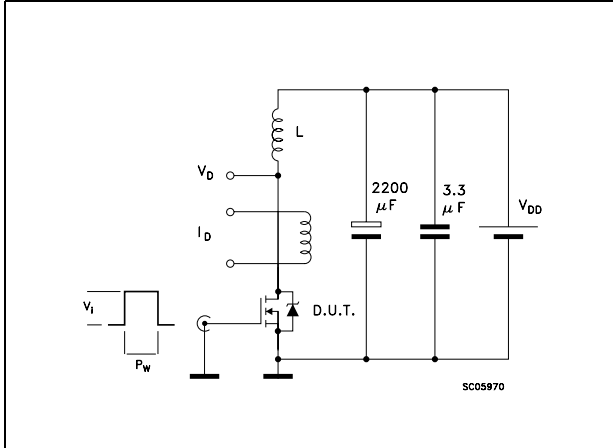


Figure 13. Unclamped inductive waveform

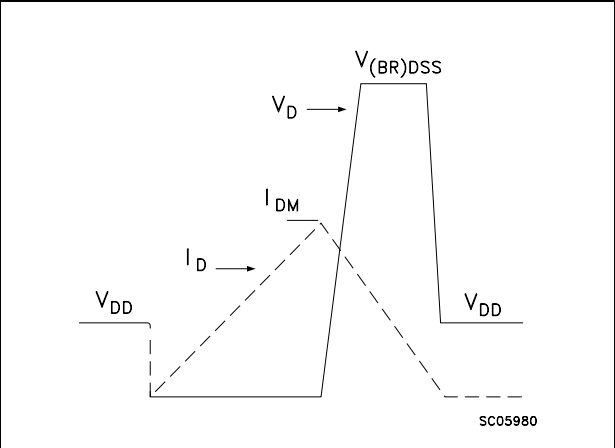


Figure 14. Switching times test circuit for resistive load

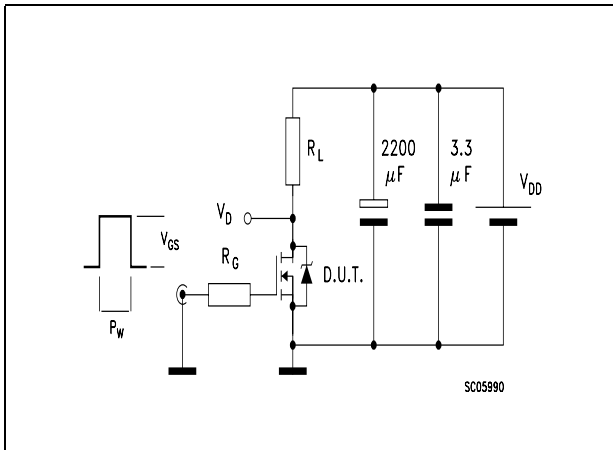


Figure 15. Gate charge test circuit

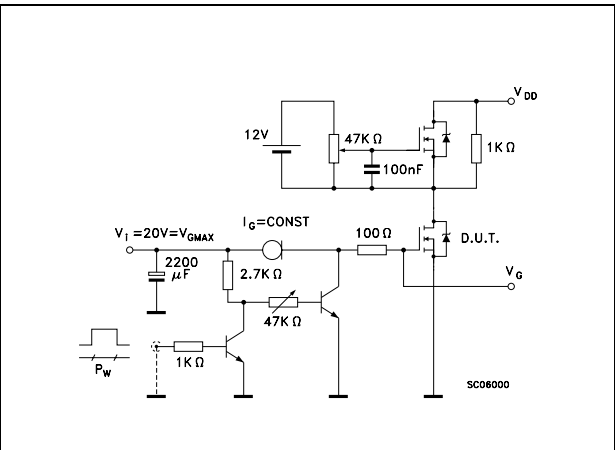
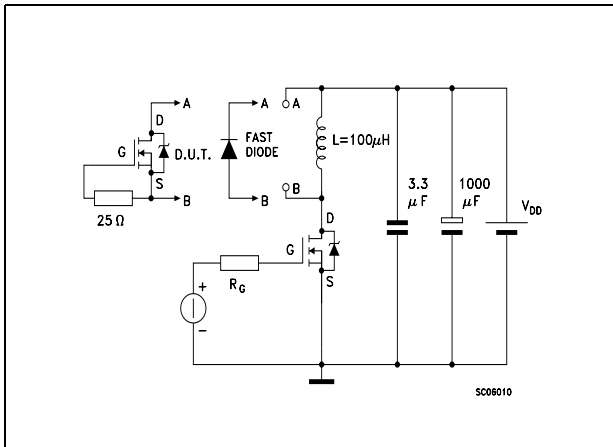


Figure 16. Test circuit for inductive load switching and diode recovery times

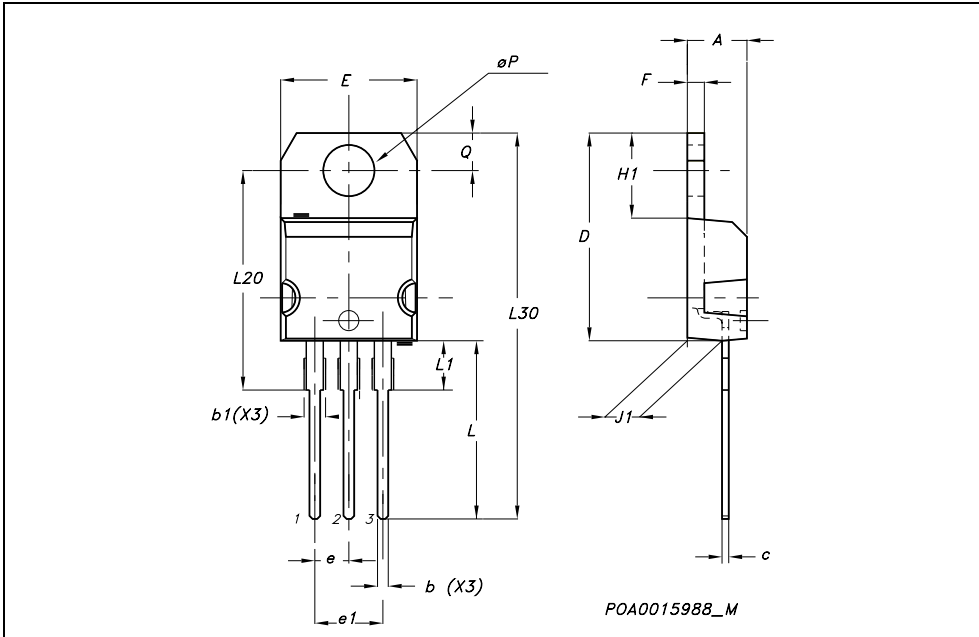


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.40 | | 4.60 | 0.173 | | 0.181 |
| b | 0.61 | | 0.88 | 0.024 | | 0.034 |
| b1 | 1.15 | | 1.70 | 0.045 | | 0.066 |
| c | 0.49 | | 0.70 | 0.019 | | 0.027 |
| D | 15.25 | | 15.75 | 0.60 | | 0.620 |
| E | 10 | | 10.40 | 0.393 | | 0.409 |
| e | 2.40 | | 2.70 | 0.094 | | 0.106 |
| e1 | 4.95 | | 5.15 | 0.194 | | 0.202 |
| F | 1.23 | | 1.32 | 0.048 | | 0.052 |
| H1 | 6.20 | | 6.60 | 0.244 | | 0.256 |
| J1 | 2.40 | | 2.72 | 0.094 | | 0.107 |
| L | 13 | | 14 | 0.511 | | 0.551 |
| L1 | 3.50 | | 3.93 | 0.137 | | 0.154 |
| L20 | | 16.40 | | | 0.645 | |
| L30 | | 28.90 | | | 1.137 | |
| øP | 3.75 | | 3.85 | 0.147 | | 0.151 |
| Q | 2.65 | | 2.95 | 0.104 | | 0.116 |



5 Revision history

Table 7. Revision history

| Date | Revision | Changes |
|-------------|-----------------|---------------------------------|
| 21-Jun-2004 | 3 | Preliminary version |
| 29-Jun-2006 | 4 | New template, no content change |

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