

LP3883 3A Fast-Response Ultra Low Dropout Linear Regulators

Check for Samples: [LP3883](#)

FEATURES

- Ultra Low Dropout Voltage (210 mV @ 3A typ)
- Low Ground Pin Current
- Load Regulation of 0.04%/A
- 60 nA Typical Quiescent Current in Shutdown
- 1.5% Output Accuracy (25°C)
- TO-220, DPAK/TO-263 Packages
- Over Temperature/over Current Protection
- -40°C to +125°C Junction Temperature Range

APPLICATIONS

- DSP Power Supplies
- Server Core and I/O Supplies
- Linear Power Supplies for PC Add-in-Cards
- Set-Top Box Power Supplies
- Microprocessor Power Supplies
- High Efficiency Linear Power Supplies
- SMPS Post-Regulators

DESCRIPTION

The LP3883 is a high-current, fast-response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220 and DPAK/TO-263 packages.

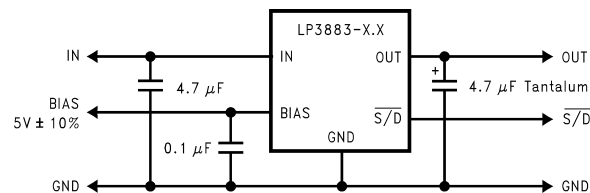
Dropout Voltage: 210 mV (typ) @ 3A load current.

Ground Pin Current: 3 mA (typ) at full load.

Shutdown Current: 60 nA (typ) when S/D pin is low.

Precision Output Voltage: 1.5% room temperature accuracy.

Typical Application Circuit



At least 4.7 µF of input and output capacitance is required for stability.

Connection Diagram

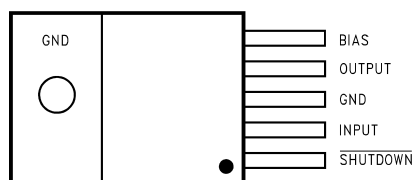


Figure 1. TO-220, Top View
See NDH0005D Package

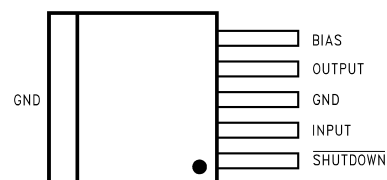


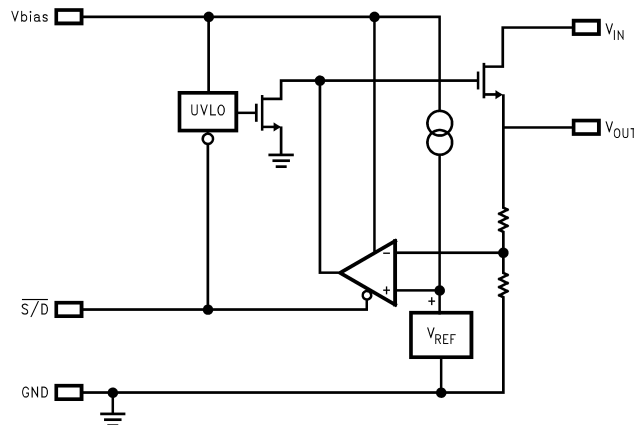
Figure 2. DPAK/TO-263, Top View
See KTT0005B Package



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Storage Temperature Range		-65°C to +150°C
Lead Temp. (Soldering, 5 seconds)		260°C
ESD Rating	Human Body Model ⁽³⁾	2 kV
	Machine Model ⁽⁴⁾	200V
Power Dissipation ⁽⁵⁾		Internally Limited
V_{IN} Supply Voltage (Survival)		-0.3V to +6V
V_{BIAS} Supply Voltage (Survival)		-0.3V to +7V
Shutdown Input Voltage (Survival)		-0.3V to +7V
I_{OUT} (Survival)		Internally Limited
Output Voltage (Survival)		-0.3V to +6V
Junction Temperature		-40°C to +150°C

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
- (4) The machine model is a 220 pF capacitor discharged directly into each pin. The machine model ESD rating of pin 5 is 100V.
- (5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. θ_{J-A} for TO-220 devices is 65°C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a θ_{J-S} value of 4°C/W can be assumed. θ_{J-A} for DDPAK/TO-263 devices is approximately 40°C/W if soldered down to a copper plane which is at least 1.5 square inches in area. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

OPERATING RATINGS

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to 5.5V
Shutdown Input Voltage	0 to +6V
I_{OUT}	3A
Operating Junction Temperature Range	-40°C to +125°C
V_{BIAS} Supply Voltage	4.5V to 6V

ELECTRICAL CHARACTERISTICS

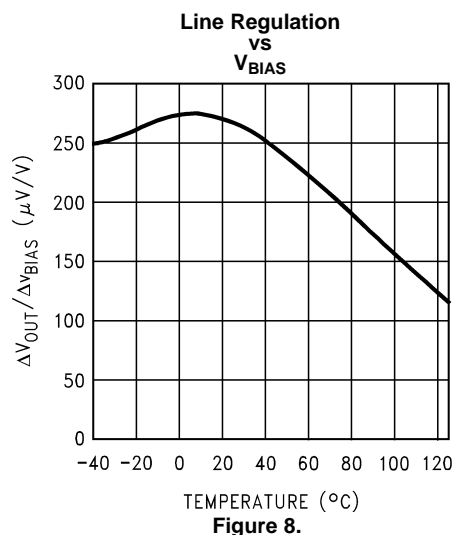
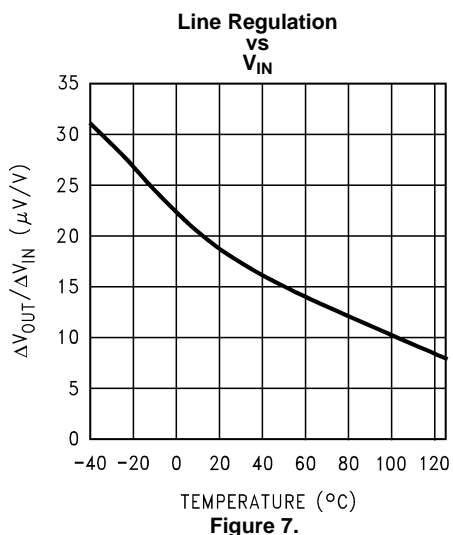
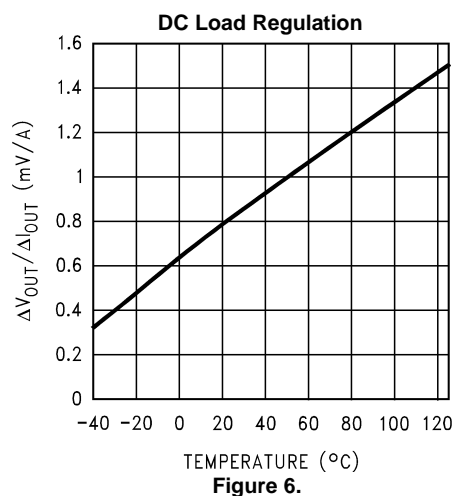
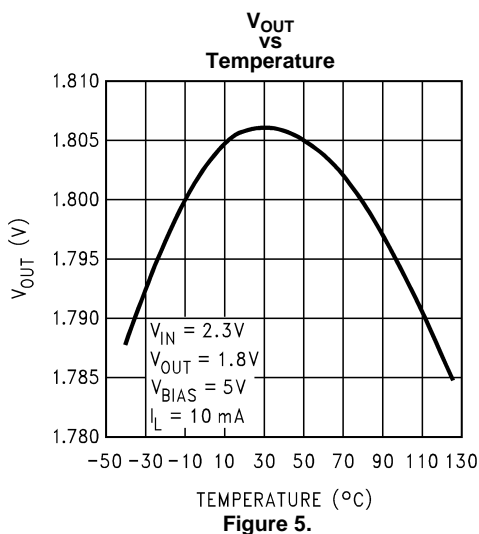
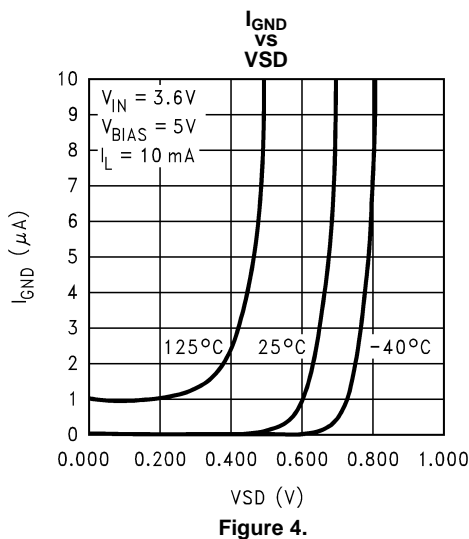
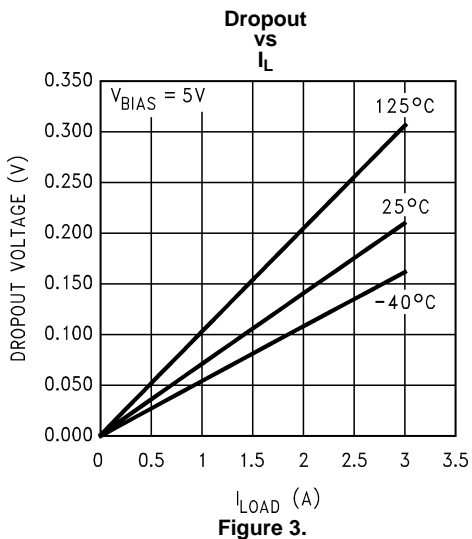
Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $V_{BIAS} = 4.5\text{V}$, $I_L = 10\text{ mA}$, $C_{IN} = C_{OUT} = 4.7\ \mu\text{F}$, $V_{S/D} = V_{BIAS}$.

Symbol	Parameter	Conditions	Typical ⁽¹⁾	MIN ⁽²⁾	MAX ⁽²⁾	Units
V_O	Output Voltage Tolerance	$10\text{ mA} < I_L < 3\text{A}$ $V_O(\text{NOM}) + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$ $4.5\text{V} \leq V_{BIAS} \leq 6\text{V}$	1.216	1.198	1.234	V
			1.5	1.478	1.522	
			1.8	1.773	1.827	
				1.186	1.246	
				1.455	1.545	
				1.746	1.854	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation ⁽³⁾	$V_O(\text{NOM}) + 1\text{V} \leq V_{IN} \leq 5.5\text{V}$	0.01			%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation ⁽⁴⁾	$10\text{ mA} < I_L < 3\text{A}$	0.04 0.06			%/A
V_{DO}	Dropout Voltage ⁽⁵⁾	$I_L = 3\text{A}$	210		270 420	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	$10\text{ mA} < I_L < 3\text{A}$	3		7 8	mA
		$\overline{V_{S/D}} \leq 0.3\text{V}$	0.03		1 30	μA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	$10\text{ mA} < I_L < 3\text{A}$	1		2 3	mA
		$\overline{V_{S/D}} \leq 0.3\text{V}$	0.03		1 30	μA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$	6			A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON	0.7	1.3		V
		Output = OFF	0.7		0.3	
$T_d(\text{OFF})$	Turn-OFF Delay	$R_{LOAD} \times C_{OUT} \ll T_d(\text{OFF})$	20			μs
$T_d(\text{ON})$	Turn-ON Delay	$R_{LOAD} \times C_{OUT} \ll T_d(\text{ON})$	15			
$\overline{I_{S/D}}$	$\overline{S/D}$ Input Current	$\overline{V_{S/D}} = 1.3\text{V}$	1			μA
		$\overline{V_{S/D}} \leq 0.3\text{V}$	-1			
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT} + 1\text{V}$, $f = 120\text{ Hz}$	80			dB
		$V_{IN} = V_{OUT} + 1\text{V}$, $f = 1\text{ kHz}$	65			
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT} + 3\text{V}$, $f = 120\text{ Hz}$	70			
		$V_{BIAS} = V_{OUT} + 3\text{V}$, $f = 1\text{ kHz}$	65			
	Output Noise Density	$f = 120\text{ Hz}$	1			$\mu\text{V}/\text{root-Hz}$
e_n	Output Noise Voltage $V_{OUT} = 1.8\text{V}$	BW = 10 Hz – 100 kHz	150			$\mu\text{V (rms)}$
		BW = 300 Hz – 300 kHz	90			

- (1) Typical numbers represent the most likely parametric norm for 25°C operation.
- (2) Limits are ensured through testing, statistical correlation, or design.
- (3) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
- (4) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
- (5) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

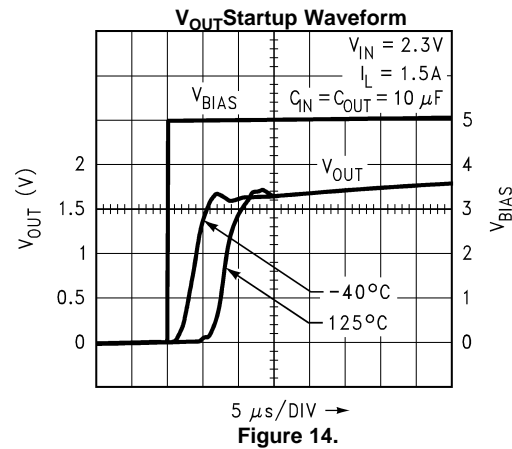
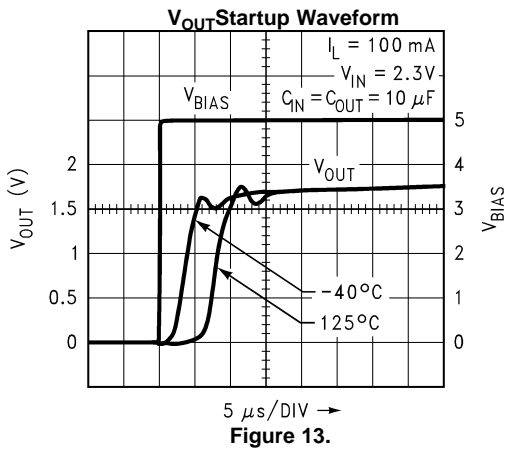
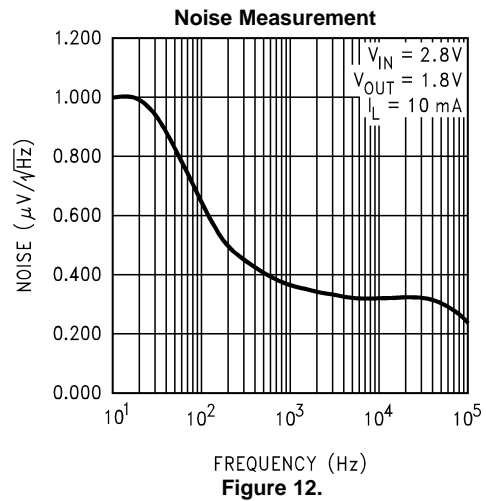
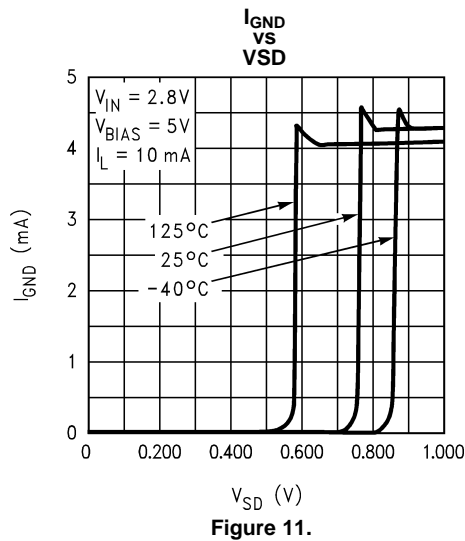
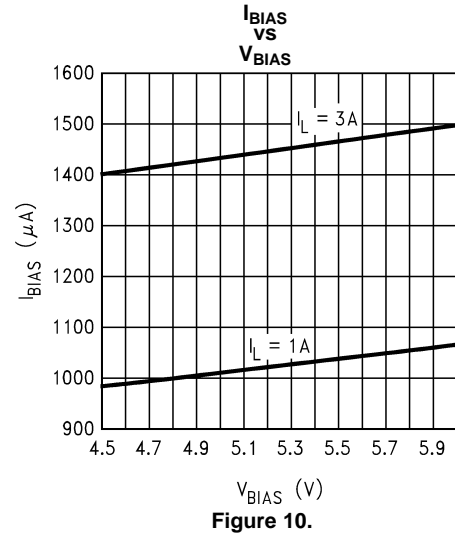
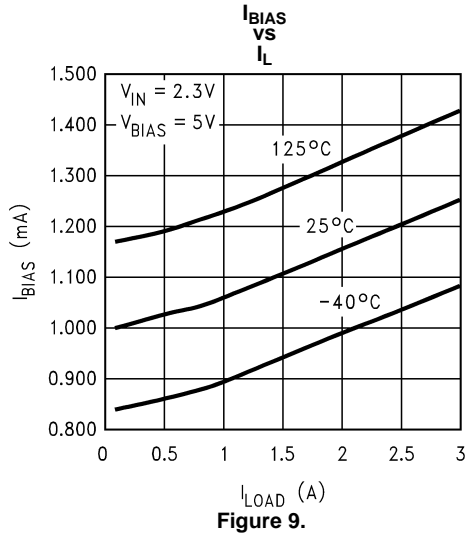
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $C_{in} = 4.7\mu\text{F}$, $\overline{S/D}$ pin is tied to V_{BIAS} , $V_{IN} = 2.2\text{V}$, $V_{OUT} = 1.8\text{V}$.



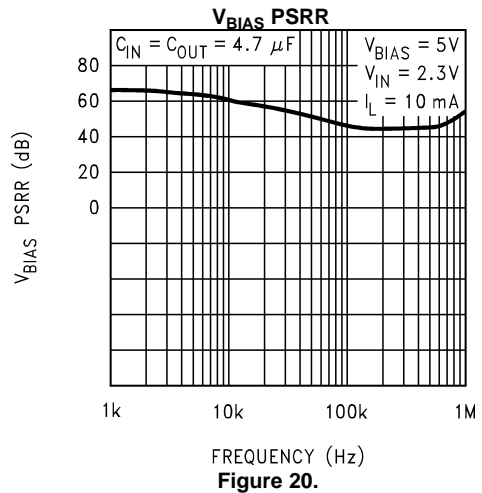
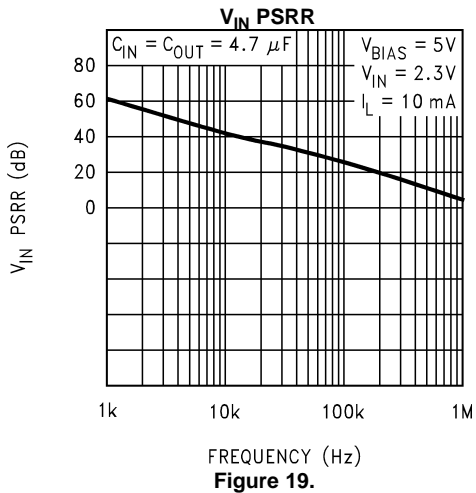
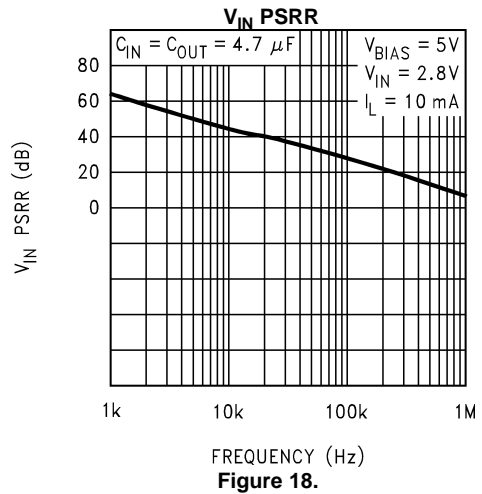
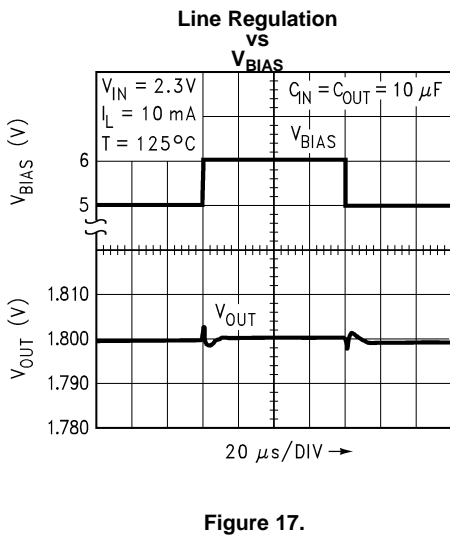
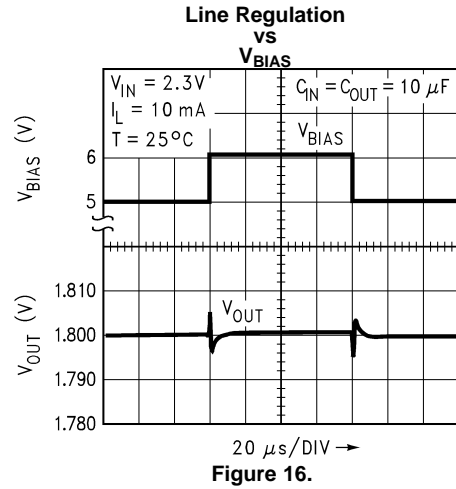
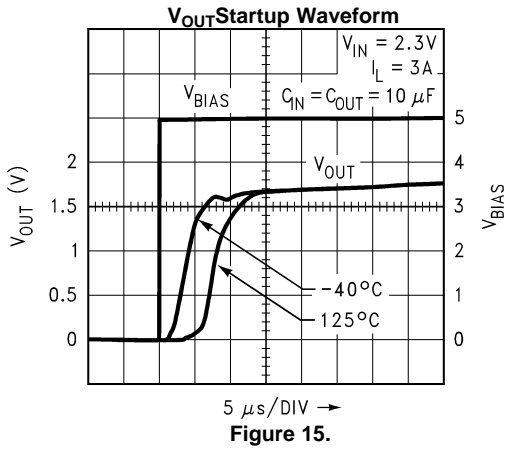
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $C_{IN} = 4.7\mu\text{F}$, $\overline{S/D}$ pin is tied to V_{BIAS} , $V_{IN} = 2.2\text{V}$, $V_{OUT} = 1.8\text{V}$.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

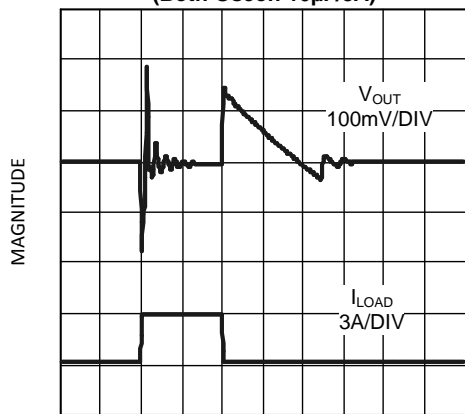
Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $C_{IN} = 4.7\mu\text{F}$, $\overline{\text{S/D}}$ pin is tied to V_{BIAS} , $V_{IN} = 2.2\text{V}$, $V_{OUT} = 1.8\text{V}$.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $C_{in} = 4.7\mu\text{F}$, $\overline{S/D}$ pin is tied to V_{BIAS} , $V_{IN} = 2.2\text{V}$, $V_{OUT} = 1.8\text{V}$.

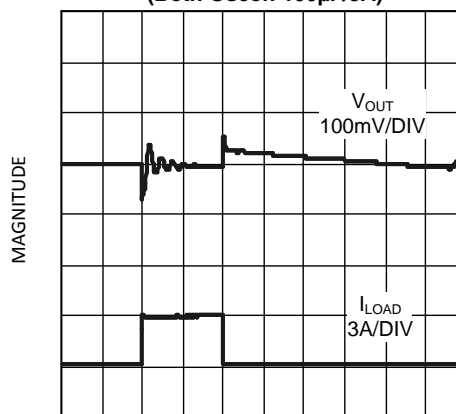
**Load Transient Response
(Both Oscon 10 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 21.

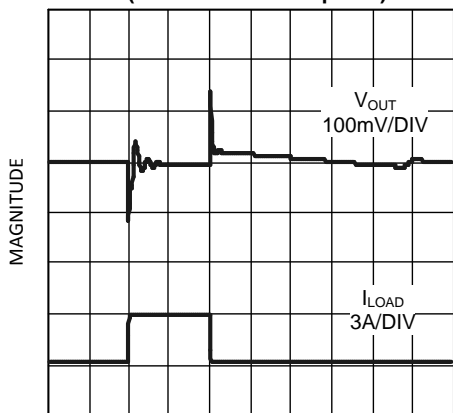
**Load Transient Response
(Both Oscon 100 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 22.

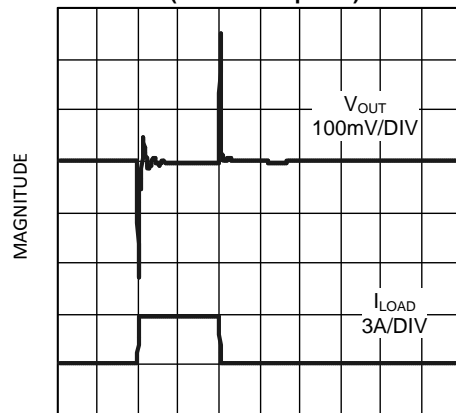
**Load Transient Response
(Both POSCAP 100 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 23.

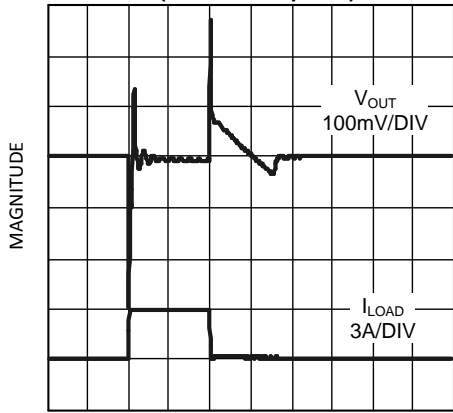
**Load Transient Response
(SANYO 150 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 24.

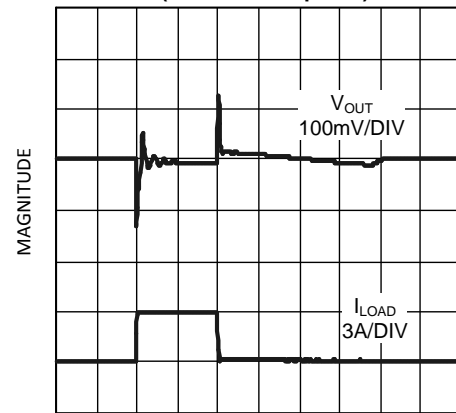
**Load Transient Response
(Tantalum 10 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 25.

**Load Transient Response
(Tantalum 100 $\mu\text{F}/3\text{A}$)**



TIME (50 μs /DIV)

Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\mu\text{F}$, $C_{in} = 4.7\mu\text{F}$, $\overline{S/D}$ pin is tied to V_{BIAS} , $V_{IN} = 2.2\text{V}$, $V_{OUT} = 1.8\text{V}$.

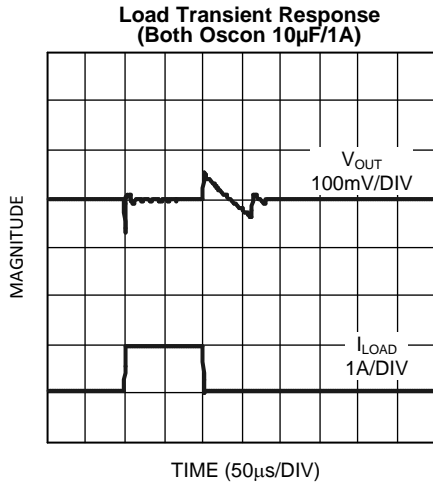


Figure 27.

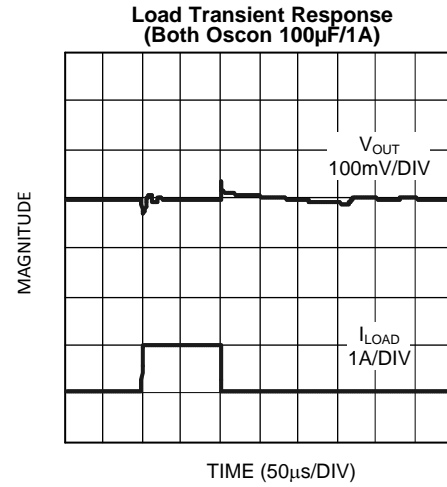


Figure 28.

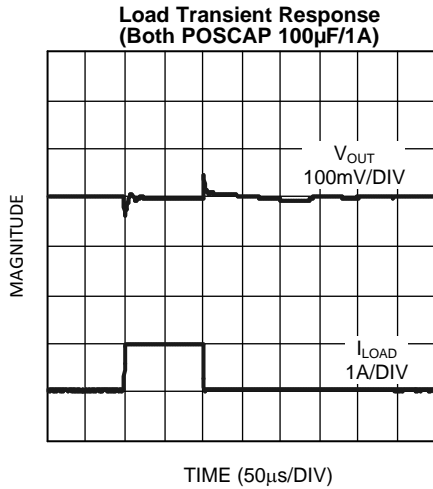


Figure 29.

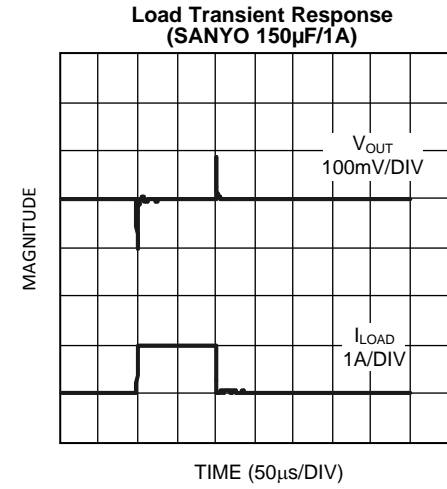


Figure 30.

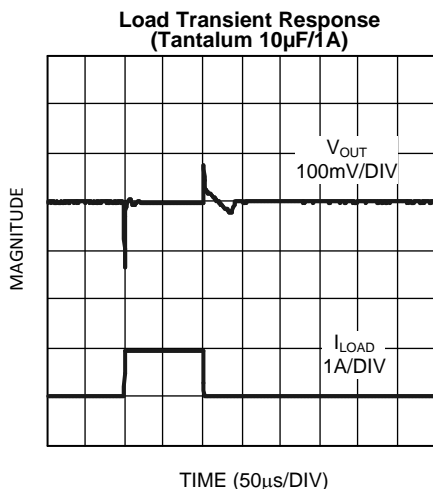


Figure 31.

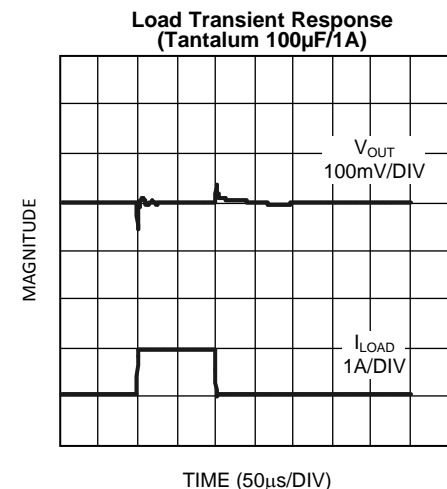


Figure 32.

APPLICATION HINTS

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

At least 4.7µF of output capacitance is required for stability (the amount of capacitance can be increased without limit). The output capacitor must be located less than 1 cm from the output pin of the IC and returned to a clean analog ground. The ESR (equivalent series resistance) of the output capacitor must be within the "stable" range as shown in the graph below over the full operating temperature range for stable operation.

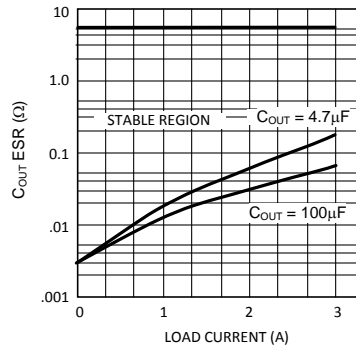


Figure 33. Minimum ESR vs Output Load Current

Tantalum capacitors are recommended for the output as their ESR is ideally suited to the part's requirements and the ESR is very stable over temperature. Aluminum electrolytics are not recommended because their ESR increases very rapidly at temperatures below 10C. Aluminum caps can only be used in applications where lower temperature operation is not required.

A second problem with Al caps is that many have ESR's which are only specified at low frequencies. The typical loop bandwidth of a linear regulator is a few hundred kHz to several MHz. If an Al cap is used for the output cap, it must be one whose ESR is specified at a frequency of 100 kHz or more.

Because the ESR of ceramic capacitors is only a few milli Ohms, they are not suitable for use as output capacitors on LP388X devices. The regulator output can tolerate ceramic capacitance totaling up to 15% of the amount of Tantalum capacitance connected from the output to ground.

OUTPUT "BYPASS" CAPACITORS

Many designers place small value "bypass" capacitors at various circuit points to reduce noise. Ceramic capacitors in the value range of about 1000pF to 0.1µF placed directly on the output of a PNP or P-FET LDO regulator can cause a loss of phase margin which can result in oscillations, even when a Tantalum output capacitor is in parallel with it. This is not unique to Texas Instruments LDO regulators, it is true of any P-type LDO regulator.

The reason for this is that PNP or P-FET regulators have a higher output impedance (compared to an NPN regulator), which results in a pole-zero pair being formed by every different capacitor connected to the output.

The zero frequency is approximately:

$$F_z = 1 / (2 \times \pi \times \text{ESR} \times C)$$

where

- ESR is the equivalent series resistance of the capacitor
- C is the value of capacitance

(1)

The pole frequency is:

$$F_p = 1 / (2 \times \pi \times R_L \times C)$$

where

- R_L is the load resistance connected to the regulator output (2)

To understand why a small capacitor can reduce phase margin: assume a typical LDO with a bandwidth of 1MHz, which is delivering 0.5A of current from a 2.5V output (which means R_L is 5 Ohms). We then place a .047 μ F capacitor on the output. This creates a pole whose frequency is:

$$F_p = 1 / (2 \times \pi \times 5 \times .047 \times 10E-6) = 677 \text{ kHz} \quad (3)$$

This pole would add close to 60 degrees of phase lag at the crossover (unity gain) frequency of 1 MHz, which would almost certainly make this regulator oscillate. Depending on the load current, output voltage, and bandwidth, there are usually values of small capacitors which can seriously reduce phase margin. If the capacitors are ceramic, they tend to oscillate more easily because they have very little internal inductance to damp it out. If bypass capacitors are used, it is best to place them near the load and use trace inductance to "decouple" them from the regulator output.

INPUT CAPACITOR

The input capacitor must be at least 4.7 μ F, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. Ceramic capacitors work best for this, but Tantalums are also very good. There is no ESR limitation on the input capacitor (the lower, the better). Aluminum electrolytics can be used, but their ESR increase very quickly at cold temperatures. They are not recommended for any application where temperatures go below about 10°C.

BIAS CAPACITOR

The 0.1 μ F capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 6V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. Pin $\overline{S/D}$ must be actively terminated through a pull-up resistor (10 k Ω to 100 k Ω) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to V_{in} if not used.

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$$

where

- I_{GND} is the operating ground current of the device (4)

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (5)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA} , can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D \tag{6}$$

These parts are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is $\geq 60\text{ }^\circ\text{C/W}$ for TO-220 package and $\geq 60\text{ }^\circ\text{C/W}$ for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC} \tag{7}$$

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W . If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. The graph below shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

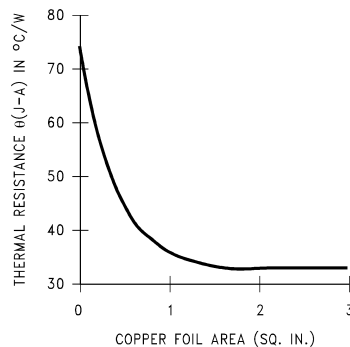


Figure 34. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W .

Figure 35 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C .

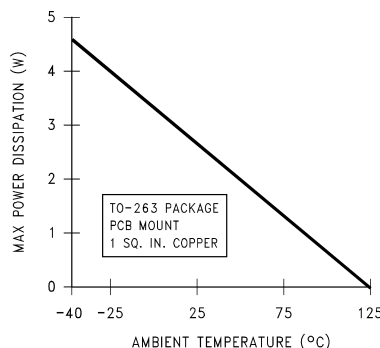


Figure 35. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F

Page

-
- Changed layout of National Data Sheet to TI format [11](#)
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3883ES-1.2	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.2	
LP3883ES-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.2	Samples
LP3883ES-1.5	NRND	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.5	
LP3883ES-1.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.5	Samples
LP3883ESX-1.2	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.2	
LP3883ESX-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3883ESX-1.2	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3883ESX-1.2/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3883ESX-1.2	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3883ESX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.