



August 2000

**QFET™**

# FQB4P40 / FQI4P40

## 400V P-Channel MOSFET

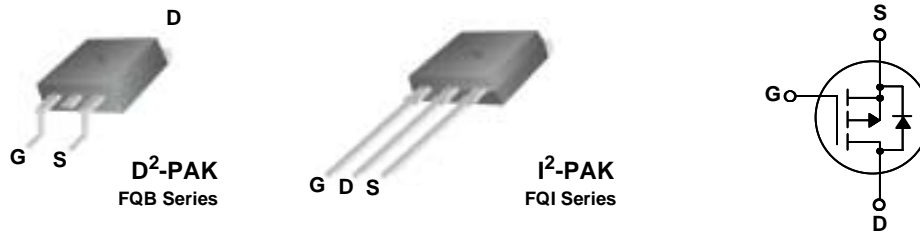
### General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

### Features

- -3.5A, -400V,  $R_{DS(on)} = 3.1\Omega @ V_{GS} = -10V$
- Low gate charge ( typical 18 nC)
- Low Crss ( typical 11 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQB4P40 / FQI4P40	Units
V <sub>DSS</sub>	Drain-Source Voltage	-400	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	-3.5	A
	- Continuous (T <sub>C</sub> = 100°C)	-2.2	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	-14	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	260	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	-3.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	8.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *	3.13	W
	Power Dissipation (T <sub>C</sub> = 25°C)	85	W
	- Derate above 25°C	0.68	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	1.47	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

\* When mounted on the minimum pad size recommended (PCB Mount)

## Elerical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.36	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -320\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

## On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.75\text{ A}$	--	2.44	3.1	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.75\text{ A}$ (Note 4)	--	2.7	--	S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	520	680	pF
$C_{oss}$	Output Capacitance		--	80	105	pF
$C_{riss}$	Reverse Transfer Capacitance		--	11	15	pF

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -200\text{ V}, I_D = -3.5\text{ A},$ $R_G = 25\ \Omega$  (Note 4, 5)	--	13	35	ns
$t_r$	Turn-On Rise Time		--	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time		--	37	85	ns
$Q_g$	Total Gate Charge	$V_{DS} = -320\text{ V}, I_D = -3.5\text{ A},$ $V_{GS} = -10\text{ V}$  (Note 4, 5)	--	18	23	nC
$Q_{gs}$	Gate-Source Charge		--	3.8	--	nC
$Q_{gd}$	Gate-Drain Charge		--	9.4	--	nC

## Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-3.5	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-14	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.5\text{ A}$	--	--	-5.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -3.5\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	260	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	1.4	--	$\mu\text{C}$

### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 37\text{ mH}, I_{AS} = -3.5\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -3.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

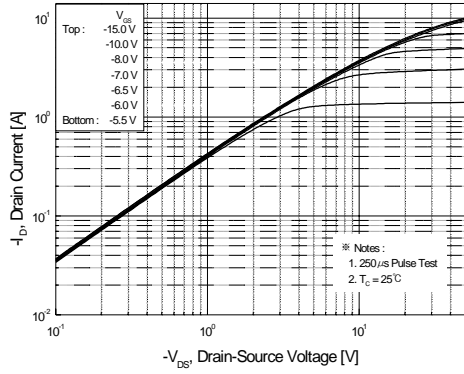


Figure 1. On-Region Characteristics

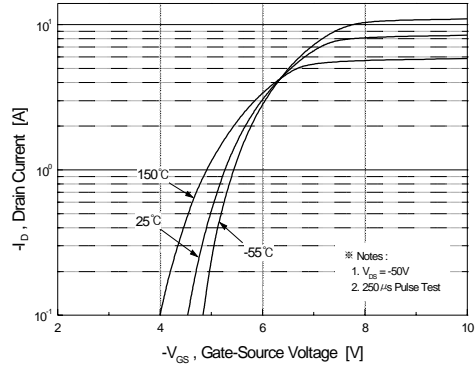


Figure 2. Transfer Characteristics

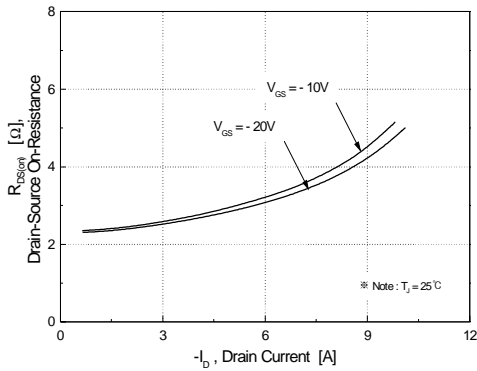


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

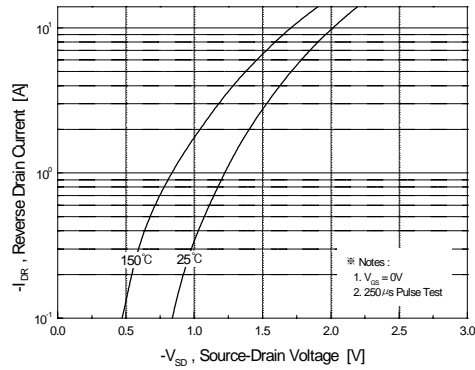


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

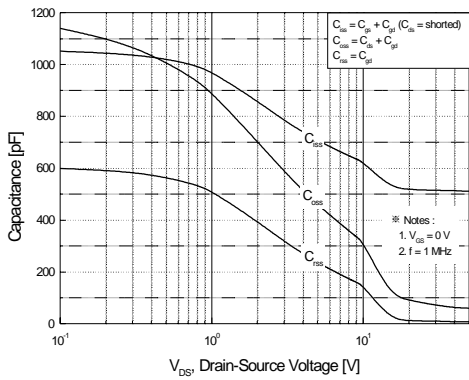


Figure 5. Capacitance Characteristics

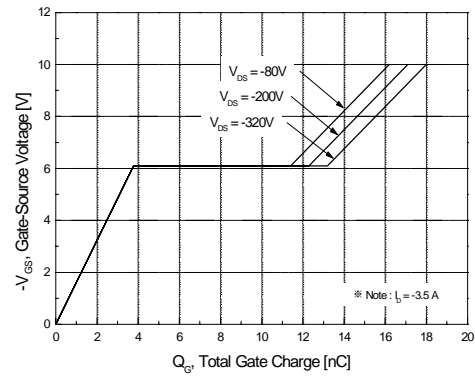
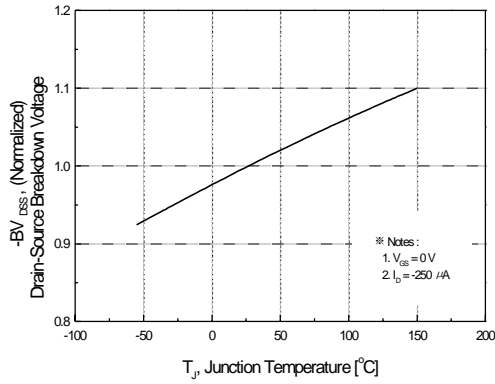
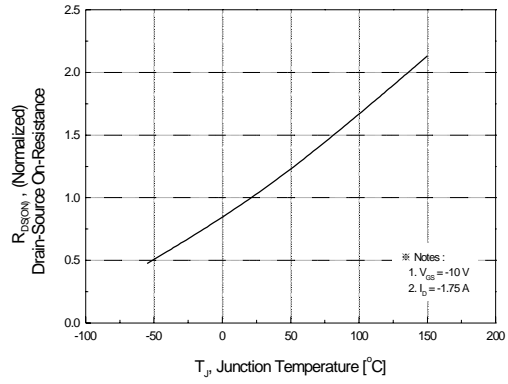


Figure 6. Gate Charge Characteristics

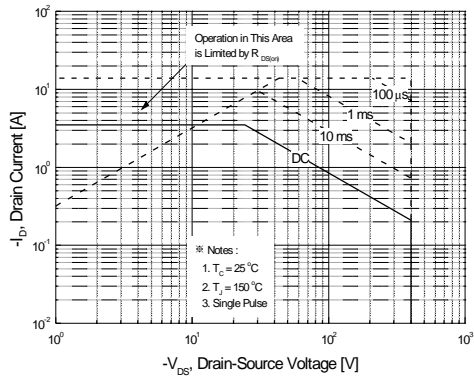
**Typical Characteristics** (Continued)



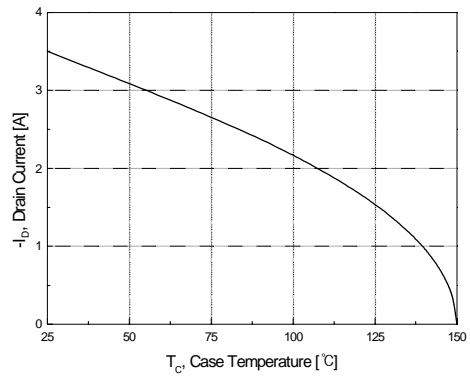
**Figure 7. Breakdown Voltage Variation vs. Temperature**



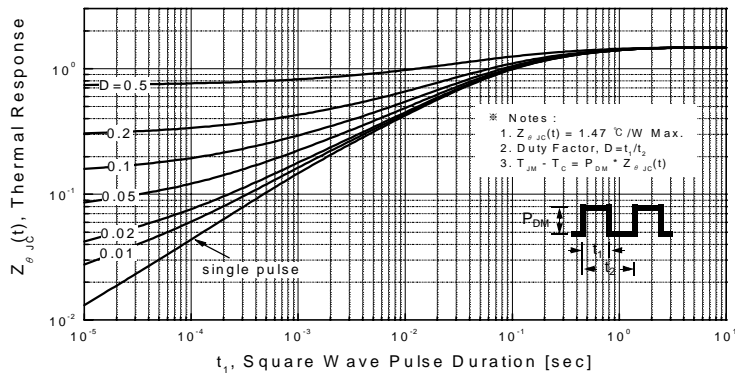
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

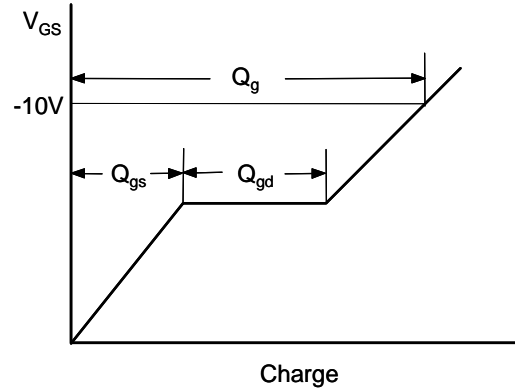
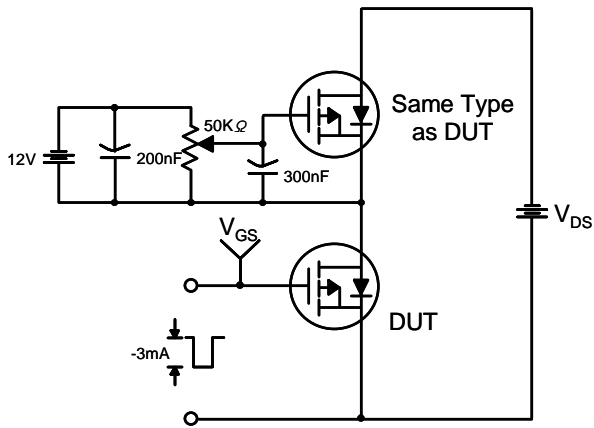


**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

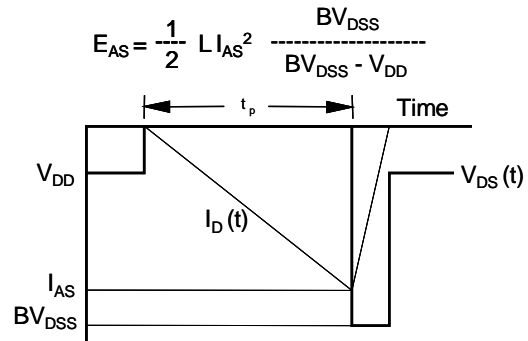
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms





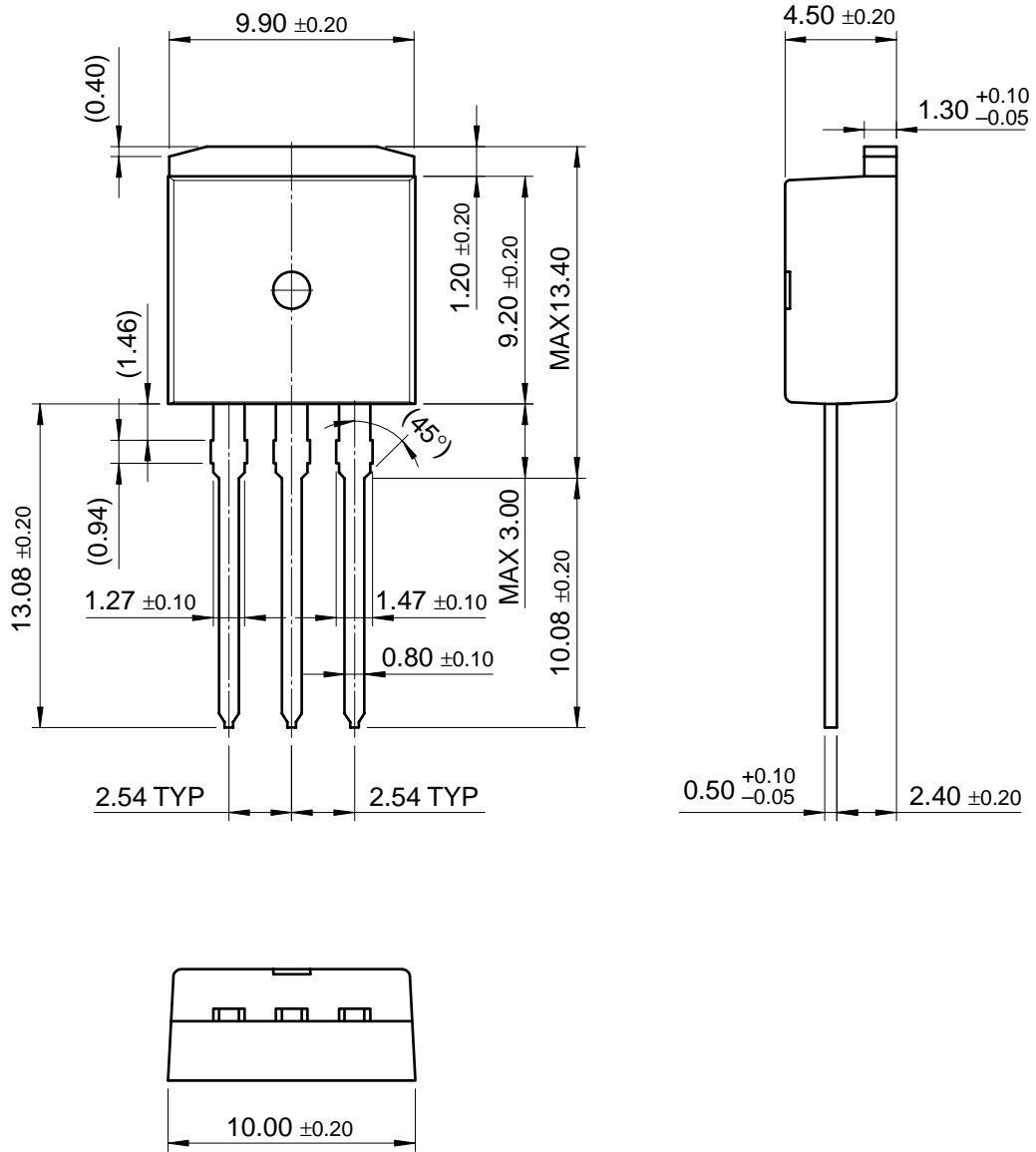
Package Dimensions

D<sup>2</sup>PAK



Package Dimensions (Continued)

I<sup>2</sup>PAK



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400V P-Channel QFET

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General description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as high efficiency switching DC/DC converters, and DC motor control.

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Features

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- Low gate charge (typical 18 nC)
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Product status/pricing/packaging

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Product	Product status	Pricing*	Package type	Leads	Packing method

FQI4P40TU	Full Production	\$0.69	TO-262(I2PAK)	3	RAIL
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\* 1,000 piece Budgetary Pricing

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