

## Features

### General

- High-performance, Low-power 32-bit ARM®-SC100™ Enhanced RISC Architecture
- Von Neumann Load / Store Architecture
  - single 32-bit Data Bus for Instructions and Data
- Memory Protection unit
- Internal Oscillator (VFO) (up to 50 MHz)
- ESD Protection to ± 2000V (± 6000V on the ISO interfaces)
- Operating Ranges: 3.3V (+/- 10%)
- Compliant with EMV Level 1, VISA PED, APACS, ZKA, Common Criteria (EAL4+), FINREAD

### Memory

- 256 bits of Key Storage (battery backup)
- 32K Bytes of internal ROM Memory (Bootstrap & Crypto library)
- 256K Bytes of Internal EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Bytes
  - 1 to 128-byte Program/Erase
  - 2 ms Program, 2 ms Erase
  - Endurance: 100,000 Write/Erase Cycles at temperature of 25 degrees C
  - 10 Years Data Retention
- 100K Bytes of Internal RAM (4KB Crypto RAM)
- up to 16M Bytes of External Memory (AT91SO100/101 only)

### Peripherals

- Page Unit to access External Memory Page (AT91SO100/101 only)
- Static Memory Controller (AT91SO100/101 only)
- Two ISO 7816 controllers with DC/DC (one of them can be multiplexed to address 4 SAM). The DC/DC converter AT83C26 is not included in the versions AT91SO100, AT91SO50 and AT91SO25. But the two ISO 7816 controllers are still available
- USB 2.0 Full Speed (8 endpoints)
- SPI Controller (up to 6Mbps) and Two Wire Interface
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
- Triple Track Magstripe Logical Interface
- 5 8-bit I/O Port Interface (LEDs, Keyboard, LCD, spare...)
- Real Time Clock (RTC) with Alarm interrupt
- System Timer including a 16-bit Counter, Watchdog and Second Counter
- Six-channel 16-bit Timer/counter
- 2-level, 28-interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Hardware AES 128-192-256
- Hardware SHA-1, SHA-256
- True Random Number Generator (RNG)
- Two CRC 16 Engines and one CRC 32 Engine (Compliant with ISO/IEC 3309)
- AdvX - Advanced crypto multiplier for cryptography and authentication (including RSA, DSA, Key Generation, ECC)

### Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Intrusion sensors (mesh and switches).
- Environmental Protection Systems (Voltage, Frequency, UV and Temperature)
- Secure Memory Management/Access Protection (MPU)
- Real time clock and battery back up
- Compliant with EMV standard, VISA PED and FINREAD



## Secure Microcontroller for Electronic Transaction Terminal / Reader

**AT91SO100/101**  
**AT91SO50/51**  
**AT91SO25**

## Summary

6514BS-SPD-10 May 07



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.



## Description

The **AT91SO100/101**, **AT91SO50/51** and the **AT91SO25** are a low-power, high-performance, SC100 32-bit microcontroller based on the ARM® enhanced RISC architecture. This new SC100 core allows the linear addressing of up to 1M bytes of code and data as well as a number of new functional and security features. A 3-level instruction pipeline allows the performance of one instruction in a single clock cycle, the SC100 achieves throughputs close to 1 MIPS per MHz. The SC100 processor employs a unique architectural strategy known as Thumb® a super reduced instruction set that is ideally suited for high volume applications with memory restrictions and applications where code density is an important factor.

The **AT91SO100/101**, **AT91SO50/51** and the **AT91SO25** have internal EEPROM that can be used as program or data memory. It also includes a ROM (for the bootstrap and crypto library and some native functions) and a large SRAM. The **AT91SO100/101** can also address up to 16Mbytes of external memory.

The **AT91SO100/101**, **AT91SO50/51** and the **AT91SO25** also comprises of strong security mechanisms and has a impressive set of cryptography features , hardware DES/TDES, hardware AES, hardware SHA-n, hardware cryptography accelerator for asymmetric algorithms (RSA, Elliptic Curve, Key generation) and a true random number generator.

The **AT91SO100/101**, **AT91SO50/51** and the **AT91SO25** includes a lot of dedicated peripherals as ISO 7816 controller and magnetic stripe card interface, as well as USB, SPI, TWI, USARTs and I/O ports.

The **AT91SO101** is a single package solution in BGA256 embedding two chips, the secure controller and the AT83C26 which physically interface with up to 2 smart cards and 3 secure access module, or 1 smart card and 4 secure access module.

The **AT91SO100** is available using the same package (BGA256) pin to pin compatible with the AT91SO101 but without the AT83C26.

The **AT91SO51** is a single package solution in BGA208 (cost effective solution) embedding two chips, the secure controller and the AT83C26 which physically interface with up to 2 smart cards and 3 secure access module, or 1 smart card and 4 secure access module. The external bus is not connected on this product.

The **AT91SO50** is available using the same package (BGA208) pin to pin compatible with the AT91SO51 but without the AT83C26. The external bus is not connected on this product.

The **AT91SO25** is a single package solution in BGA144 (low cost solution) embedding one chip, the secure controller **only**. The external bus is also not connected on this product.

**Figure 1.** Block Diagram (Secure controller)

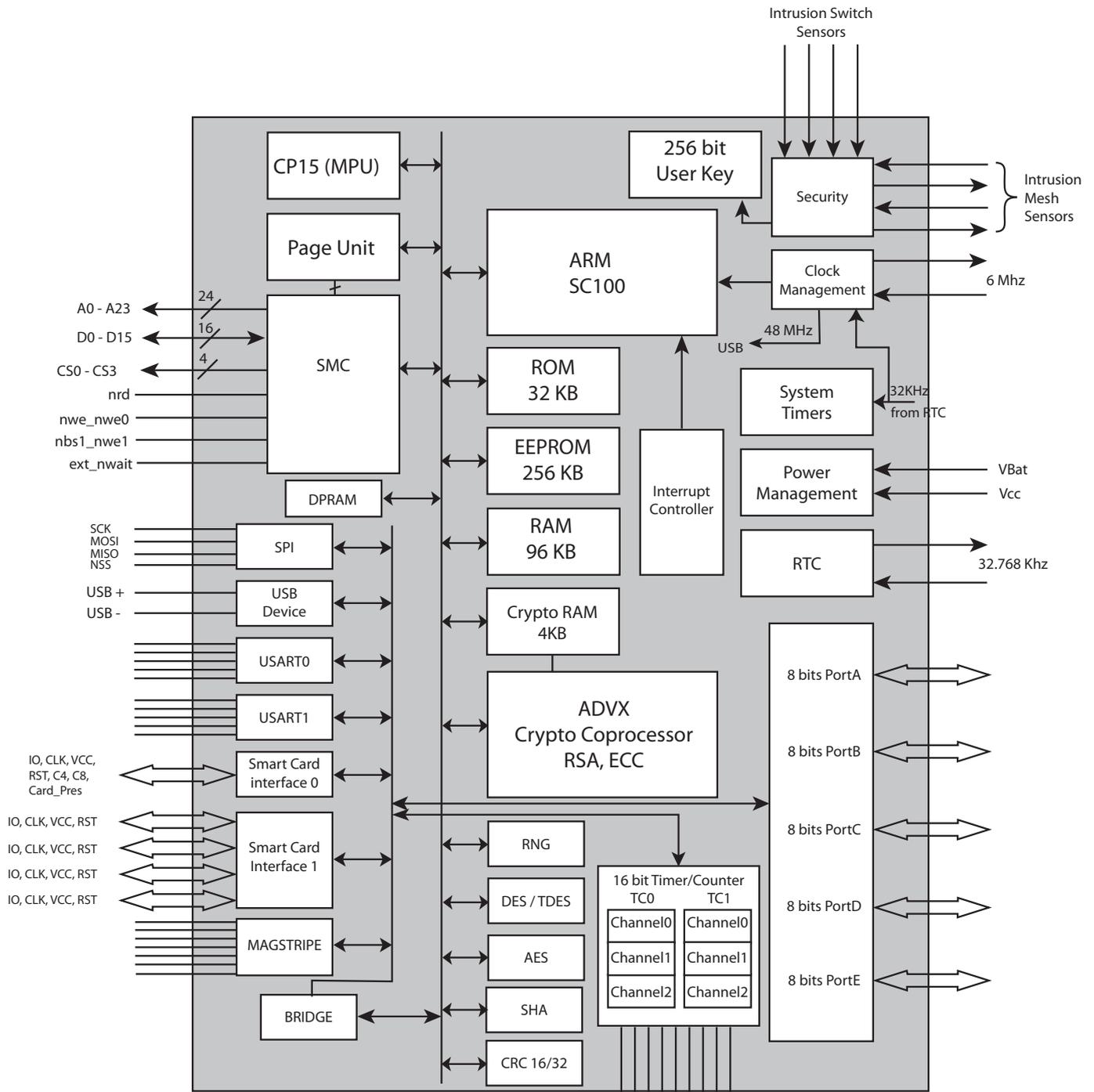
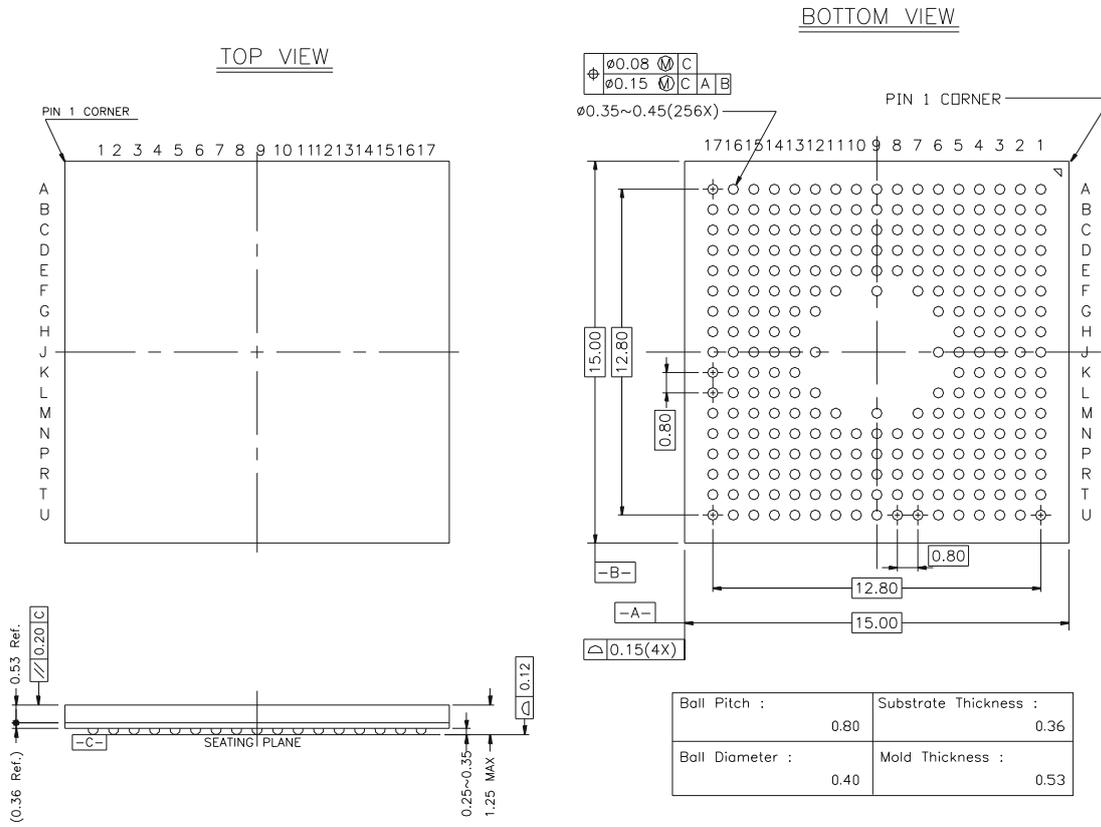


Figure 2. BGA256 (AT91SO100/101)



All dimensions are in mm

Figure 3. BGA208 (AT91SO50/51)

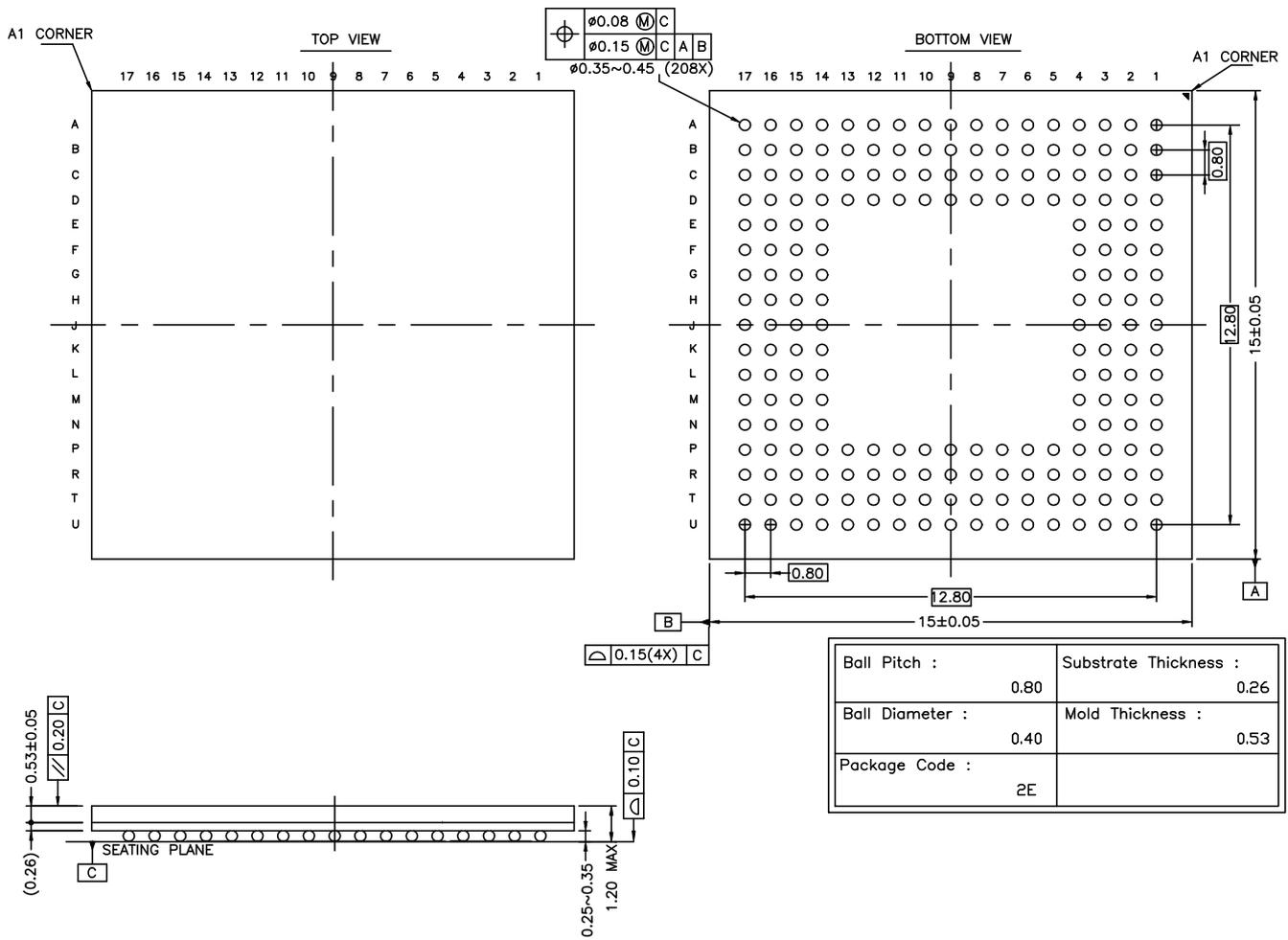
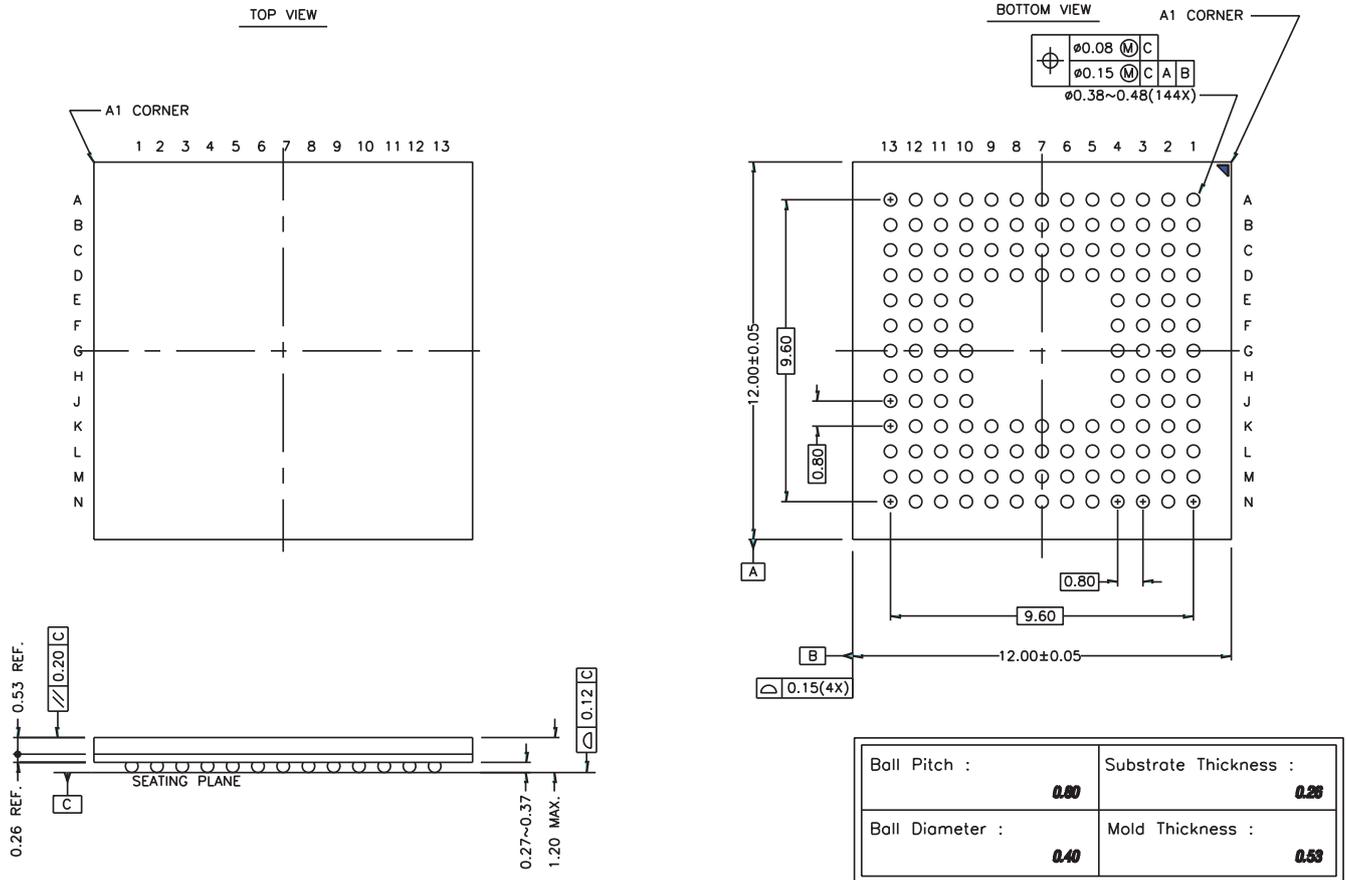


Figure 4. BGA144 (AT91SO25)





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## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

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