PART NUMBER DATA SHEET

EQRE13A2J-100.000M

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REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 2, 2017)

Lead Free COMPLIANT | EU RoHS 2011/65 + 2015/863 COMPLIANT | China RoHS COMPLIANT | REACH 174 SVHC COMPLIANT

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Regulatory Compliance standards are subject to updates by governing bodies. Click the badges to download the latest compliance docs for this part number directly from Ecliptek.

DRC CONFLICT FREE

ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVDS (DS) 3.3Vdc 6 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 100.000MHz ±100ppm over 0°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	100.000MHz
Frequency Tolerance/Stability	±100ppm Maximum over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance (at 25°C), Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Aging at 25°C	±3ppm Maximum First Year
Supply Voltage	3.3Vdc ±5%
Input Current	30mA Maximum
Output Voltage Logic High (Voh)	1.43Vdc Typical, 1.6Vdc Maximum
Output Voltage Logic Low (Vol)	1.1Vdc Typical, 0.9Vdc Minimum
Differential Output Error (dVod)	50mV Maximum
Differential Output Voltage (Vod)	247mV Minimum, 330mV Typical, 454mV Maximum
Offset Voltage (Vos)	1.125V Minimum, 1.250V Typical, 1.375V Maximum
Rise/Fall Time	400pSec Maximum (Measured at 20% to 80% of Waveform)
Duty Cycle	50 ±5(%) (Measured at 50% of Waveform)
Offset Error (dVos)	50mV Maximum
Load Drive Capability	100 Ohms Between Output and Complementary Output
Output Logic Type	LVDS
Phase Noise	All Values are Typical -50dBc/Hz at 10Hz Offset -82dBc/Hz at 100Hz Offset -116dBc/Hz at 1kHz Offset -138dBc/Hz at 10kHz Offset -144dBc/Hz at 100kHz Offset -149dBc/Hz at 1MHz Offset -155dBc/Hz at 10MHz Offset -155dBc/Hz at 20MHz Offset
Output Control Function	Standby (on Pad 1)
Output Control Input Voltage Logic High (Vih)	70% of Vdd Minimum or No Connect to Enable Output and Complementary Output
Output Control Input Voltage Logic Low (Vil)	30% of Vdd Maximum to Disable Output and Complementary Output (High Impedance)
Standby Output Enable Time	10mSec Maximum
Standby Output Disable Time	200nSec Maximum
Standby Current	10µA Maximum (Without Load)
RMS Phase Jitter	200fSec Maximum (Fj=12kHz to 20MHz (Random))
Period Jitter (Deterministic)	0.2pSec Typical
Period Jitter (Random)	1.0pSec Typical
Period Jitter (One Sigma)	1.5pSec Typical
Period Jitter (tp-p)	40pSec Maximum
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

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EQRE13A2J-100.000M

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ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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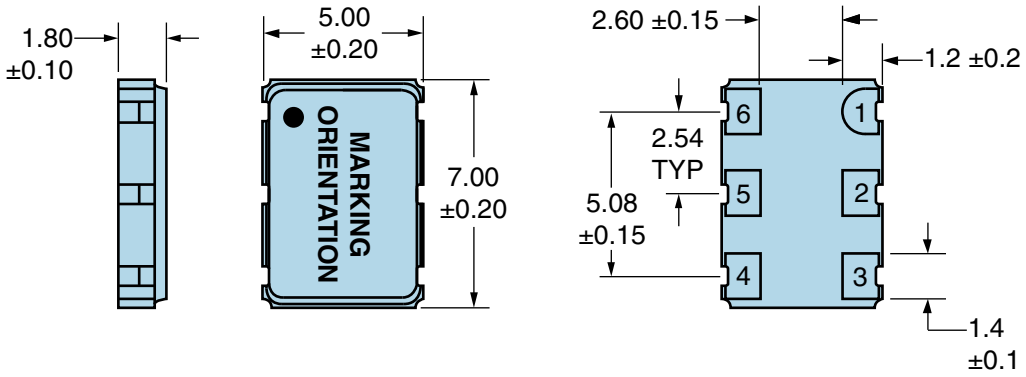
MECHANICAL DIMENSIONS (all dimensions in millimeters)

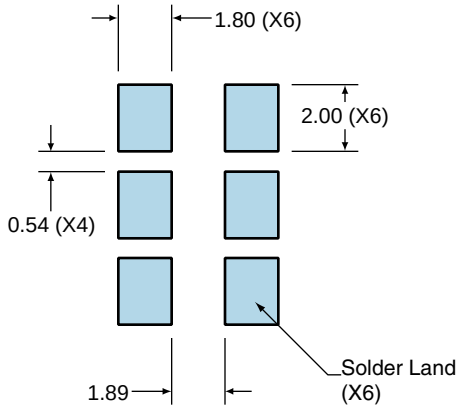


PIN	CONNECTION
1	Standby
2	No Connect
3	Case Ground
4	Output
5	Complementary Output
6	Supply Voltage

LINE	MARKING
1	**ECLIPTEK**
2	**100.00M**
3	**XXXXX** *XXXXX=Ecliptek Manufacturing Identifier*

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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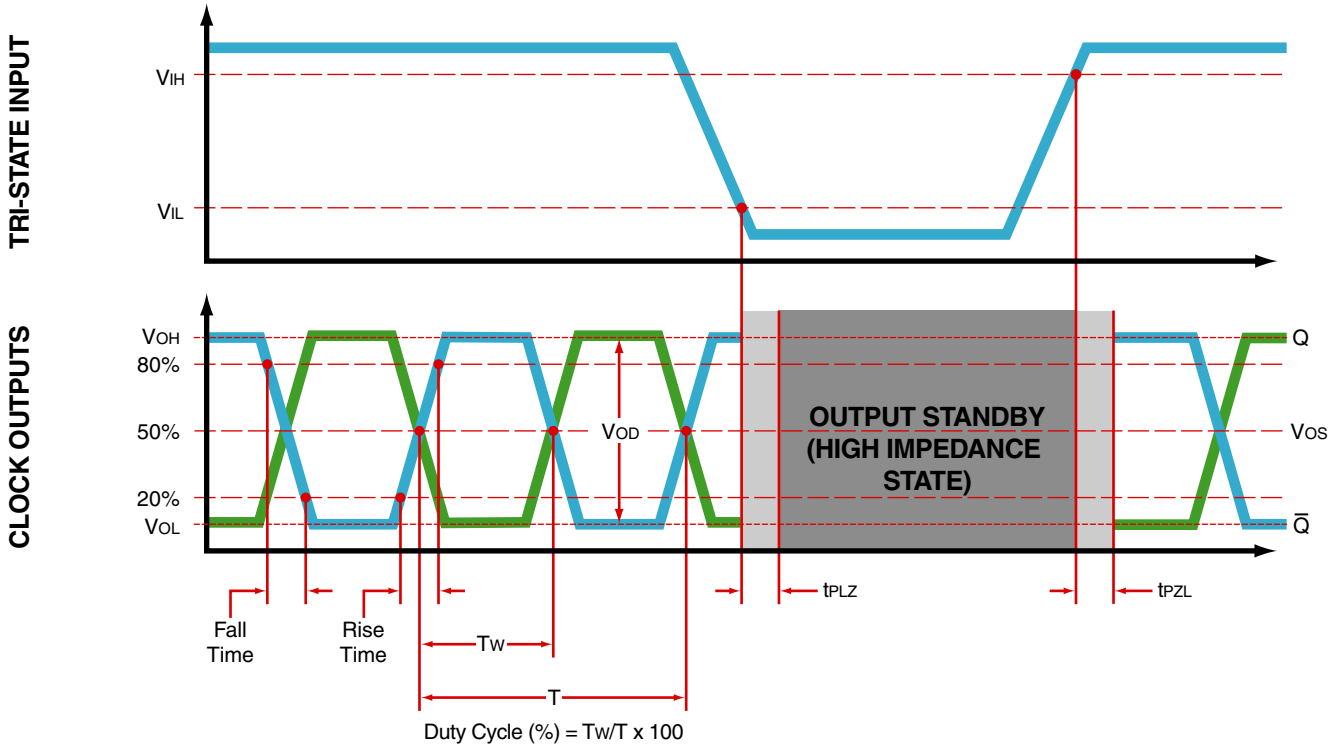
OUTPUT WAVEFORM & TIMING DIAGRAM



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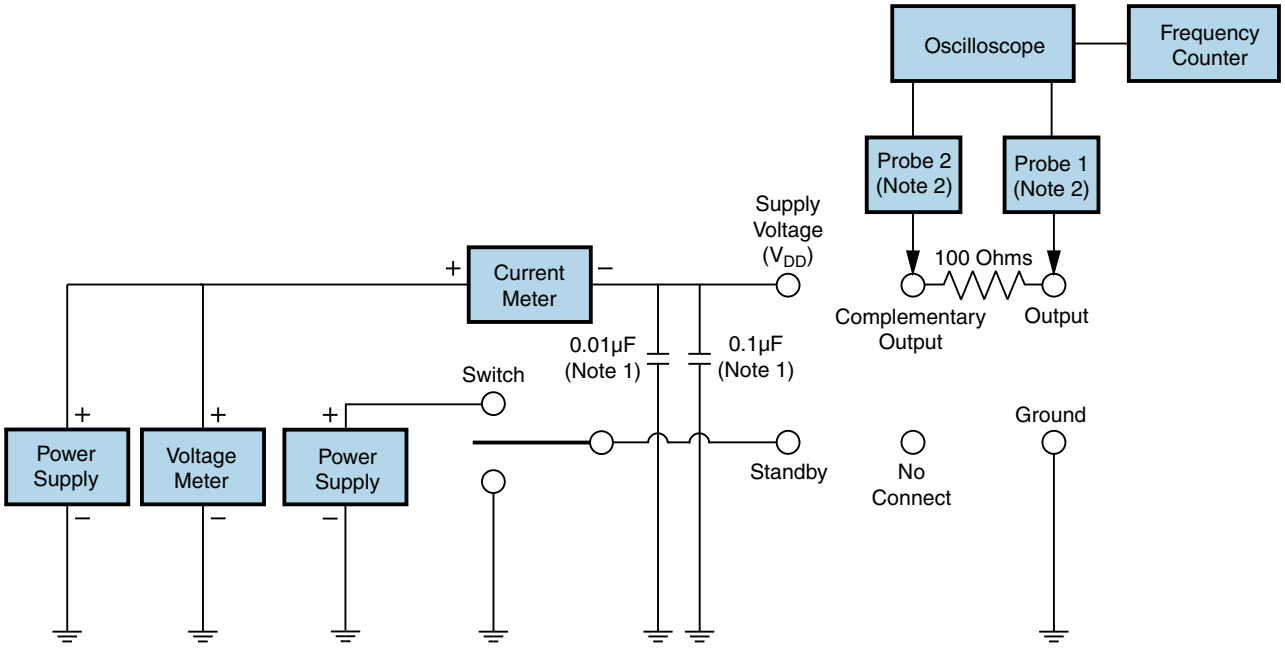
Test Circuit for Standby (Pad 1) and Complementary Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>500MHz) passive probe is recommended.
Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.

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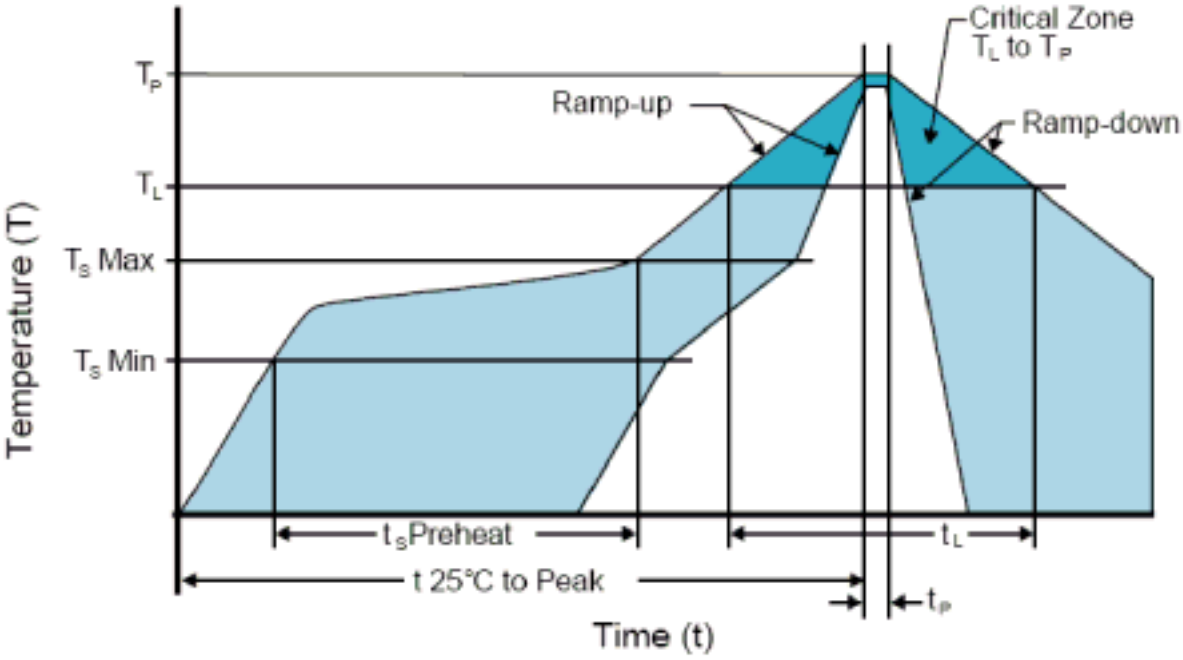
Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T_S MAX to T_L (Ramp-up Rate)	3°C/Second Maximum
Preheat	
- Temperature Minimum (T_S MIN)	150°C
- Temperature Typical (T_S TYP)	175°C
- Temperature Maximum (T_S MAX)	200°C
- Time (t_S MIN)	60 - 180 Seconds
Ramp-up Rate (T_L to T_P)	3°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	217°C
- Time (t_L)	60 - 150 Seconds
Peak Temperature (T_P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T_P Target)	250°C +0/-5°C
Time within 5°C of actual peak (t_p)	20 - 40 Seconds
Ramp-down Rate	6°C/Second Maximum
Time 25°C to Peak Temperature (t)	8 Minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

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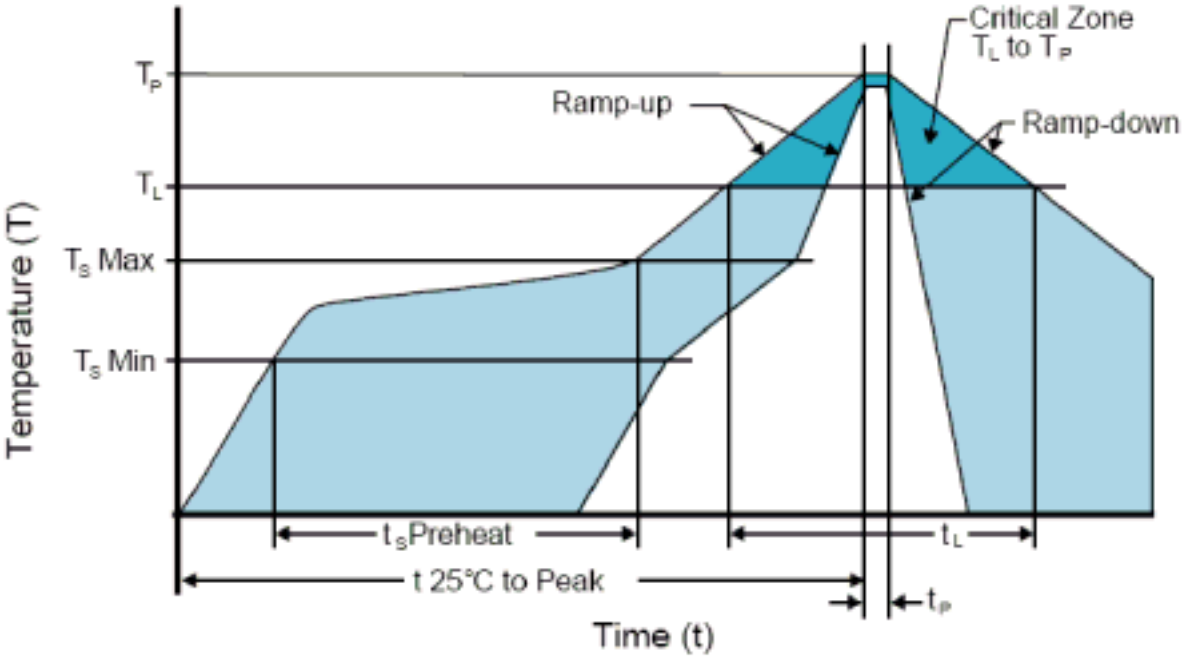

Low Temperature Infrared/Convection 240°C

TS MAX to TL (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (TS MIN)	N/A
- Temperature Typical (TS TYP)	150°C
- Temperature Maximum (TS MAX)	N/A
- Time (tS MIN)	60 - 120 Seconds
Ramp-up Rate (TL to TP)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (TL)	150°C
- Time (tL)	200 Seconds Maximum
Peak Temperature (TP)	240°C Maximum
Target Peak Temperature (TP Target)	240°C Maximum 2 Times / 230°C Maximum 1 Time
Time within 5°C of actual peak (tP)	10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to body of device.)

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to body of device.)

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